DAQ

DAQCard™-6062E User Manual

Multifunction I/O Card for PCMCIA

NATIONAL INSTRUMENTS™

April 2000 Edition
Part Number 322641A-01

Worldwide Technical Support and Product Information

www.ni.com

National Instruments Corporate Headquarters

11500 North Mopac Expressway Austin, Texas 78759-3504 USA Tel: 512 794 0100

Worldwide Offices

Australia 03 9879 5166, Austria 0662 45 79 90 0, Belgium 02 757 00 20, Brazil 011 284 5011,
Canada (Calgary) 403 274 9391, Canada (Ontario) 905 785 0085, Canada (Québec) 514 694 8521,
China 0755 3904939, Denmark 45 76 26 00, Finland 09 725 725 11, France 01 48 14 24 24,
Germany 089 741 31 30, Greece 30 1 42 96 427, Hong Kong 2645 3186, India 91805275406,
Israel 03 6120092, Italy 02 413091, Japan 03 5472 2970, Korea 02 596 7456, Mexico (D.F.) 5 280 7625,
Mexico (Monterrey) 8 357 7695, Netherlands 0348 433466, New Zealand 09 914 0488, Norway 32 27 73 00,
Poland 0 22 528 94 06, Portugal 351 1 726 9011, Singapore 2265886, Spain 91 640 0085,
Sweden 08 587 895 00, Switzerland 056 200 51 51, Taiwan 02 2528 7227, United Kingdom 01635 523545

For further support information, see the *Technical Support Resources* appendix. To comment on the documentation, send e-mail to techpubs@ni.com

Important Information

Warranty

The DAQCard-6062E is warranted against defects in materials and workmanship for a period of one year from the date of shipment, as evidenced by receipts or other documentation. National Instruments will, at its option, repair or replace equipment that proves to be defective during the warranty period. This warranty includes parts and labor.

The media on which you receive National Instruments software are warranted not to fail to execute programming instructions, due to defects in materials and workmanship, for a period of 90 days from date of shipment, as evidenced by receipts or other documentation. National Instruments will, at its option, repair or replace software media that do not execute programming instructions if National Instruments receives notice of such defects during the warranty period. National Instruments does not warrant that the operation of the software shall be uninterrupted or error free.

A Return Material Authorization (RMA) number must be obtained from the factory and clearly marked on the outside of the package before any equipment will be accepted for warranty work. National Instruments will pay the shipping costs of returning to the owner parts which are covered by warranty.

National Instruments believes that the information in this document is accurate. The document has been carefully reviewed for technical accuracy. In the event that technical or typographical errors exist, National Instruments reserves the right to make changes to subsequent editions of this document without prior notice to holders of this edition. The reader should consult National Instruments if errors are suspected. In no event shall National Instruments be liable for any damages arising out of or related to this document or the information contained in it.

EXCEPT AS SPECIFIED HEREIN, NATIONAL INSTRUMENTS MAKES NO WARRANTIES, EXPRESS OR IMPLIED, AND SPECIFICALLY DISCLAIMS ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. CUSTOMER'S RIGHT TO RECOVER DAMAGES CAUSED BY FAULT OR NEGLIGENCE ON THE PART OF NATIONAL INSTRUMENTS SHALL BE LIMITED TO THE AMOUNT THERETOFORE PAID BY THE CUSTOMER. NATIONAL INSTRUMENTS WILL NOT BE LIABLE FOR DAMAGES RESULTING FROM LOSS OF DATA, PROFITS, USE OF PRODUCTS, OR INCIDENTAL OR CONSEQUENTIAL DAMAGES, EVEN IF ADVISED OF THE POSSIBILITY THEREOF. This limitation of the liability of National Instruments will apply regardless of the form of action, whether in contract or tort, including negligence. Any action against National Instruments must be brought within one year after the cause of action accrues. National Instruments shall not be liable for any delay in performance due to causes beyond its reasonable control. The warranty provided herein does not cover damages, defects, malfunctions, or service failures caused by owner's failure to follow the National Instruments installation, operation, or maintenance instructions; owner's modification of the product; owner's abuse, misuse, or negligent acts; and power failure or surges, fire, flood, accident, actions of third parties, or other events outside reasonable control.

Copyright

Trademarks

WARNING REGARDING USE OF NATIONAL INSTRUMENTS PRODUCTS

(1) NATIONAL INSTRUMENTS PRODUCTS ARE NOT DESIGNED WITH COMPONENTS AND TESTING FOR A LEVEL OF RELIABILITY SUITABLE FOR USE IN OR IN CONNECTION WITH SURGICAL IMPLANTS OR AS CRITICAL COMPONENTS IN ANY LIFE SUPPORT SYSTEMS WHOSE FAILURE TO PERFORM CAN REASONABLY BE EXPECTED TO CAUSE SIGNIFICANT INJURY TO A HUMAN.

(2) IN ANY APPLICATION, INCLUDING THE ABOVE, RELIABILITY OF OPERATION OF THE SOFTWARE PRODUCTS CAN BE IMPAIRED BY ADVERSE FACTORS, INCLUDING BUT NOT LIMITED TO FLUCTUATIONS IN ELECTRICAL POWER SUPPLY, COMPUTER HARDWARE MALFUNCTIONS, COMPUTER OPERATING SYSTEM SOFTWARE FITNESS, FITNESS OF COMPILERS AND DEVELOPMENT SOFTWARE USED TO DEVELOP AN APPLICATION, INSTALLATION ERRORS, SOFTWARE AND HARDWARE COMPATIBILITY PROBLEMS, MALFUNCTIONS OR FAILURES OF ELECTRONIC MONITORING OR CONTROL DEVICES, TRANSIENT FAILURES OF ELECTRONIC SYSTEMS (HARDWARE AND/OR SOFTWARE), UNANTICIPATED USES OR MISUSES, OR ERRORS ON THE PART OF THE USER OR APPLICATIONS DESIGNER (ADVERSE FACTORS SUCH AS THESE ARE HEREAFTER COLLECTIVELY TERMED "SYSTEM FAILURES"). ANY APPLICATION WHERE A SYSTEM FAILURE WOULD CREATE A RISK OF HARM TO PROPERTY OR PERSONS (INCLUDING THE RISK OF BODILY INJURY AND DEATH) SHOULD NOT BE RELIANT SOLELY UPON ONE FORM OF ELECTRONIC SYSTEM DUE TO THE RISK OF SYSTEM FAILURE. TO AVOID DAMAGE, INJURY, OR DEATH, THE USER OR APPLICATION DESIGNER MUST TAKE REASONABLY PRUDENT STEPS TO PROTECT AGAINST SYSTEM FAILURES, INCLUDING BUT NOT LIMITED TO BACK-UP OR SHUT DOWN MECHANISMS. BECAUSE EACH END-USER SYSTEM IS CUSTOMIZED AND DIFFERS FROM NATIONAL INSTRUMENTS' TESTING PLATFORMS AND BECAUSE A USER OR APPLICATION DESIGNER MAY USE NATIONAL INSTRUMENTS PRODUCTS IN COMBINATION WITH OTHER PRODUCTS IN A MANNER NOT EVALUATED OR CONTEMPLATED BY NATIONAL INSTRUMENTS, THE USER OR APPLICATION DESIGNER IS ULTIMATELY RESPONSIBLE FOR VERIFYING AND VALIDATING THE SUITABILITY OF NATIONAL INSTRUMENTS PRODUCTS WHENEVER NATIONAL INSTRUMENTS PRODUCTS ARE INCORPORATED IN A SYSTEM OR APPLICATION, INCLUDING, WITHOUT LIMITATION, THE APPROPRIATE DESIGN, PROCESS AND SAFETY LEVEL OF SUCH SYSTEM OR APPLICATION.

Compliance

FCC/Canada Radio Frequency Interference Compliance*

Determining FCC Class

The Federal Communications Commission (FCC) has rules to protect wireless communications from interference. The FCC places digital electronics into two classes. These classes are known as Class A (for use in industrial-commercial locations only) or Class B (for use in residential or commercial locations). Depending on where it is operated, this product could be subject to restrictions in the FCC rules. (In Canada, the Department of Communications (DOC), of Industry Canada, regulates wireless interference in much the same way.)

Digital electronics emit weak signals during normal operation that can affect radio, television, or other wireless products. By examining the product you purchased, you can determine the FCC Class and therefore which of the two FCC/DOC Warnings apply in the following sections. (Some products may not be labeled at all for FCC; if so, the reader should then assume these are Class A devices.)

FCC Class A products only display a simple warning statement of one paragraph in length regarding interference and undesired operation. Most of our products are FCC Class A. The FCC rules have restrictions regarding the locations where FCC Class A products can be operated.

FCC Class B products display either a FCC ID code, starting with the letters **EXN**, or the FCC Class B compliance mark that appears as shown here on the right.

Consult the FCC web site `http://www.fcc.gov` for more information.

FCC/DOC Warnings

This equipment generates and uses radio frequency energy and, if not installed and used in strict accordance with the instructions in this manual and the CE Mark Declaration of Conformity**, may cause interference to radio and television reception. Classification requirements are the same for the Federal Communications Commission (FCC) and the Canadian Department of Communications (DOC).

Changes or modifications not expressly approved by National Instruments could void the user's authority to operate the equipment under the FCC Rules.

Class A

Federal Communications Commission

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Canadian Department of Communications

This Class A digital apparatus meets all requirements of the Canadian Interference-Causing Equipment Regulations.

Cet appareil numérique de la classe A respecte toutes les exigences du Règlement sur le matériel brouilleur du Canada.

Class B

Federal Communications Commission

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.

- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Canadian Department of Communications

This Class B digital apparatus meets all requirements of the Canadian Interference-Causing Equipment Regulations.

Cet appareil numérique de la classe B respecte toutes les exigences du Règlement sur le matériel brouilleur du Canada.

European Union - Compliance to EEC Directives

Readers in the EU/EEC/EEA must refer to the Manufacturer's Declaration of Conformity (DoC) for information** pertaining to the CE Mark compliance scheme. The Manufacturer includes a DoC for most every hardware product except for those bought for OEMs, if also available from an original manufacturer that also markets in the EU, or where compliance is not required as for electrically benign apparatus or cables.

* Certain exemptions may apply in the USA, see FCC Rules §15.103 **Exempted devices**, and §15.105(c). Also available in sections of CFR 47.

** The CE Mark Declaration of Conformity will contain important supplementary information and instructions for the user or installer.

Conventions

The following conventions are used in this manual.

< >	Angle brackets containing numbers separated by an ellipsis represent a range of values associated with a bit, port, or signal name (for example, ACH<0..7> stands for ACH0 through ACH7).
	This icon denotes a note, which alerts you to important information.
	This icon denotes a warning, which advises you of precautions to take to avoid being electrically shocked.
bold	Bold text denotes items that you must select or click on in the software, such as menu items and dialog box options. Bold text also denotes parameter names.
italic	Italic text denotes variables, emphasis, a cross reference, or an introduction to a key concept. This font also denotes text that is a placeholder for a word or value that you must supply.
`monospace`	Text in this font denotes text or characters that you should enter from the keyboard, sections of code, programming examples, and syntax examples. This font is also used for the proper names of disk drives, paths, directories, programs, subprograms, subroutines, device names, functions, operations, variables, filenames and extensions, and code excerpts.
NI-DAQ	NI-DAQ refers to NI-DAQ software unless otherwise noted.

Contents

Chapter 1
Introduction

Chapter 2
Installation and Configuration

Chapter 3
Hardware Overview

Chapter 4
Signal Connections

Chapter 5
Calibration

Appendix A
Specifications

Appendix B
Optional Cable Connector Descriptions

Appendix C
Common Questions

Appendix D
Technical Support Resources

Glossary

Index

Figures

Tables

1

Introduction

This manual describes the electrical and mechanical aspects of the DAQCard-6062E and contains information concerning its operation and programming..

This chapter describes the DAQCard-6062E, lists what you need to get started, explains how to unpack your DAQCard-6062E, and describes the optional software and optional equipment.

About the DAQCard-6062E

Thank you for buying a National Instruments DAQCard-6062E. The DAQCard-6062E is a multifunction analog, digital, and timing I/O card for computers equipped with Type II PCMCIA slots. This card features a 12-bit ADC, two 12-bit DACs, eight lines of TTL-compatible digital I/O, and two 24-bit counter/timers for timing I/O.

The DAQCard-6062E uses the National Instruments DAQ-STC system timing controller for time-related functions. The DAQ-STC consists of three timing groups that control analog input, analog output, and general-purpose counter/timer functions. These groups include a total of seven 24-bit and three 16-bit counters and a maximum timing resolution of 50 ns.

The DAQCard-6062E can interface to an SCXI system so that you can acquire over 3,000 analog signals from thermocouples, RTDs, strain gauges, voltage sources, and current sources. You can also acquire or generate digital signals for communication and control. SCXI is the instrumentation front end for plug-in DAQ boards.

Detailed specifications for the DAQCard-6062E are in Appendix A, *Specifications*.

What You Need to Get Started

To set up and use your DAQCard-6062E, you will need the following:

- ❑ A DAQCard-6062E card
- ❑ *DAQCard-6062E User Manual*
- ❑ One of the following software packages and documentation:
  - NI-DAQ
  - LabVIEW
  - LabWindows/CVI
- ❑ Your computer

Unpacking

Your DAQCard-6062E is shipped in an antistatic vinyl box. When you are not using your DAQCard-6062E, store it in this box. Because your DAQCard-6062E is enclosed in a fully shielded case, no additional electrostatic precautions are necessary. However, for your own safety and to protect your DAQCard-6062E, never attempt to touch the connector pins.

Software Programming Choices

You can choose from several options when programming your National Instruments DAQ and SCXI hardware. You can use LabVIEW, LabWindows/CVI, NI-DAQ, or register-level programming.

LabVIEW and LabWindows/CVI Application Software

LabVIEW features interactive graphics, a state-of-the-art user interface, and a powerful graphical programming language. The LabVIEW Data Acquisition VI Library, a series of VIs for using LabVIEW with National Instruments DAQ hardware, is included with LabVIEW. The LabVIEW Data Acquisition VI Library is functionally equivalent to the NI-DAQ software.

LabWindows/CVI features interactive graphics, a state-of-the-art user interface, and uses the ANSI standard C programming language. The LabWindows/CVI Data Acquisition Library, a series of functions

for using LabWindows/CVI with National Instruments DAQ hardware, is included with the NI-DAQ software kit. The LabWindows/CVI Data Acquisition Library is functionally equivalent to the NI-DAQ software.

Using LabVIEW or LabWindows/CVI software will greatly reduce the development time for your data acquisition and control application.

NI-DAQ Driver Software

The NI-DAQ driver software is included with most National Instruments DAQ hardware. NI-DAQ has an extensive library of functions that you can call from your application programming environment. These functions allow you to use all features of your DAQCard-6062E device.

NI-DAQ addresses many of the complex issues between the computer and the DAQ hardware such as programming interrupts. NI-DAQ maintains a consistent software interface among its different versions so that you can change platforms with minimal modifications to your code. Whether you are using LabVIEW, LabWindows/CVI, or other programming languages, your application uses the NI-DAQ driver software, as illustrated in Figure 1-1.

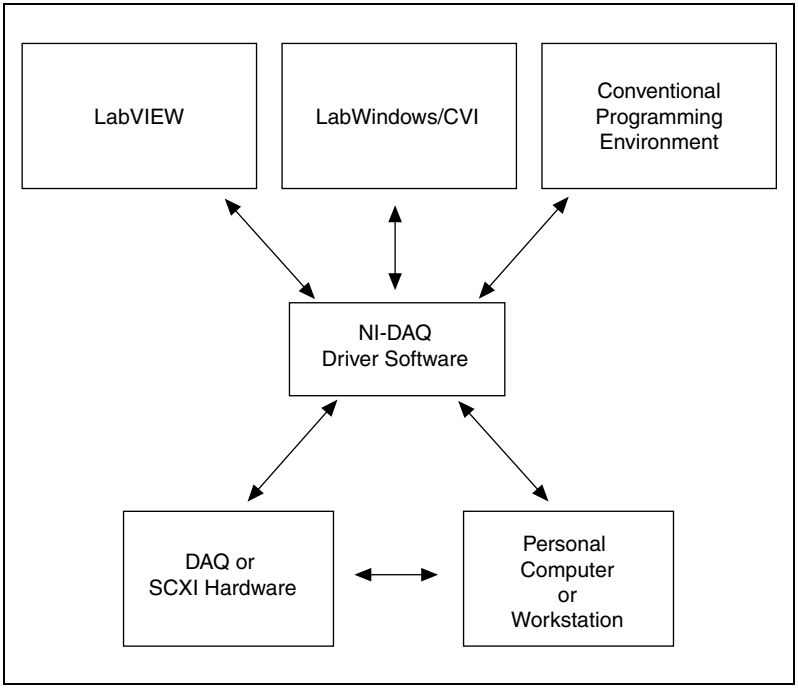


Figure 1-1. The Relationship between the Programming Environment, NI-DAQ, and Your Hardware

You can use your DAQCard-6062E, together with other PCI, PXI, PC, AT, DAQCard, and DAQPad Series DAQ and SCXI hardware, with NI-DAQ software.

Optional Equipment

National Instruments offers a variety of products to use with your DAQCard-6062E, including cables, connector blocks, and other accessories, as follows:

- Cables and cable assemblies, shielded and ribbon
- Connector blocks, shielded and unshielded, with 50- and 68-pin screw terminals
- SCXI modules and accessories for isolating, amplifying, exciting, and multiplexing signals for relays and analog output. With SCXI, you can condition and acquire up to 3,072 channels.

- Low channel-count signal conditioning modules, cards, and accessories, including conditioning for strain gauges and RTDs, simultaneous sample-and-hold circuitry, and relays.

For more specific information about these products, refer to your National Instruments catalog or call the office nearest you.

Custom Cabling

National Instruments offers cables and accessories for you to prototype your application or to use if you frequently change DAQCard-6062E interconnections.

If you want to develop your own cable, however, the following guidelines may be useful:

- For the analog input signals, shielded twisted-pair wires for each analog input pair yield the best results, assuming that you use differential inputs. Tie the shield for each signal pair to the ground reference at the source.
- You should route the analog lines separately from the digital lines.
- When using a cable shield, use separate shields for the analog and digital halves of the cable. Failure to do so results in noise coupling into the analog signals from transient digital signals.

National Instruments recommends the SHC68-68-EP cable. The SHC68-68-EP cable is a shielded, latching 68-pin cable that mates to your DAQCard I/O connector. This cable connects to the DAQCard 68-position VHDCI connector on one end and terminates with a 68-pin 0.050 series D-type connector on the other end.

2

Installation and Configuration

This chapter explains how to install and configure a DAQCard-6062E.

Installation

Note You should install your driver software before installing your hardware. Refer to your NI-DAQ release notes for software installation instructions.

There is one basic step to installing a DAQCard-6062E.

1. Insert the DAQCard-6062E and attach the I/O cable.

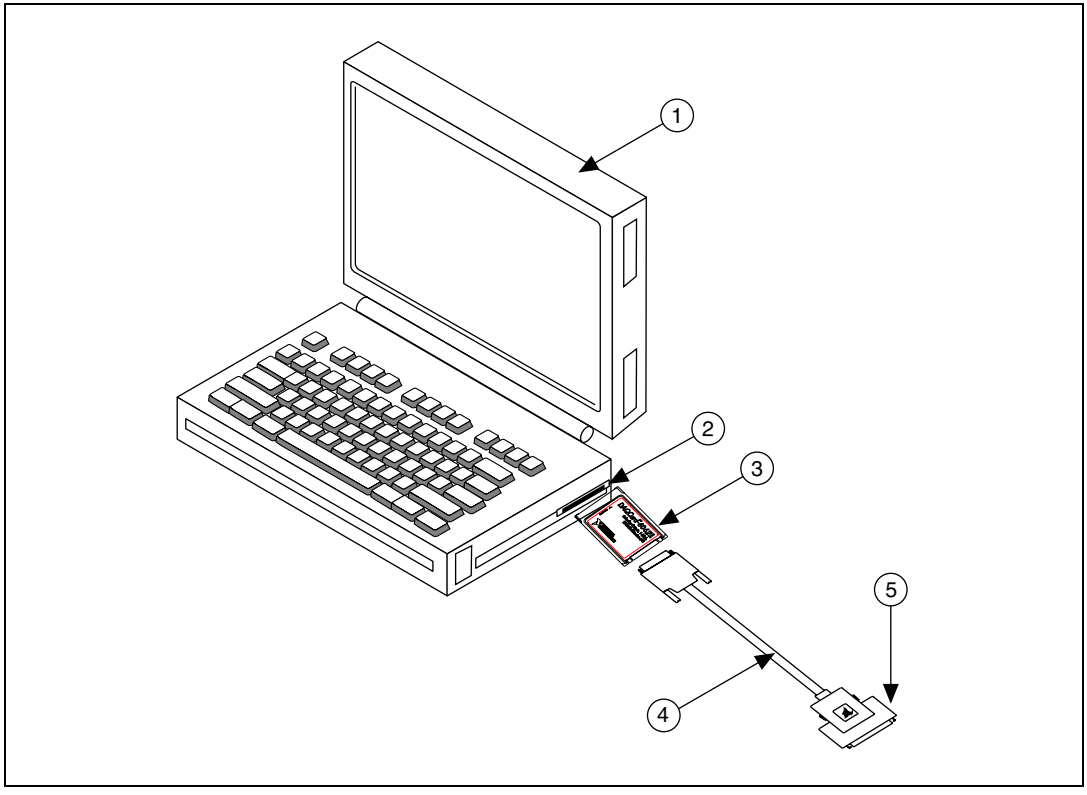
   The DAQCard-6062E has two connectors—a 68-pin PCMCIA bus connector on one end and a 68-pin I/O connector on the other end. Insert the PCMCIA bus connector into any available Type II PCMCIA slot until the connector is seated firmly. Notice that the DAQCard-6062E and I/O cable are both keyed so that the cable can be inserted only one way.

   Be careful not to put strain on the I/O cable when inserting it into and removing it from the DAQCard-6062E. Always grasp the cable by the connector you are plugging or unplugging. *Never* pull directly on the I/O cable to unplug it from the DAQCard-6062E.

   Your DAQCard-6062E can be connected to 68- and 50-pin accessories. You can use the SHC68-68-EP to connect directly to 68-pin accessories, or you can use the SHC68-68-EP in conjunction with the 68M-50F adapter to connect to 50-pin accessories. See Appendix B, *Optional Cable Connector Descriptions*, for more information.

The DAQCard-6062E is now installed. You are ready to make the appropriate connections to the I/O connector cable as described in Chapter 4, *Signal Connections*.

Figure 2-1 shows an example of a typical configuration.



1	Portable Computer	3	DAQCard-6062E	5	I/O Signals
2	PCMCIA Socket	4	SHC68-68-EP		

Figure 2-1. A Typical Configuration for the DAQCard-6062E

Configuration

Your DAQCard-6062E is completely software configurable. Refer to the Measurement & Automation Explorer (located on your PC desktop) online help file for information to configure your DAQCard-6062E.

If you are using NI-DAQ, refer to your NI-DAQ release notes to install your driver software. Find the installation section for your operating system and follow the instructions given there.

If you are using LabVIEW, refer to your LabVIEW release notes to install your application software. After you have installed LabVIEW, refer to the NI-DAQ release notes and follow the instructions given there for your operating system and LabVIEW.

If you are using LabWindows/CVI, refer to your LabWindows/CVI release notes to install your application software. After you have installed LabWindows/CVI, refer to the NI-DAQ release notes and follow the instructions given there for your operating system and LabWindows/CVI.

3

Hardware Overview

This chapter presents an overview of the hardware functions on your DAQCard-6062E.

Figure 3-1 shows the block diagram for the DAQCard-6062E.

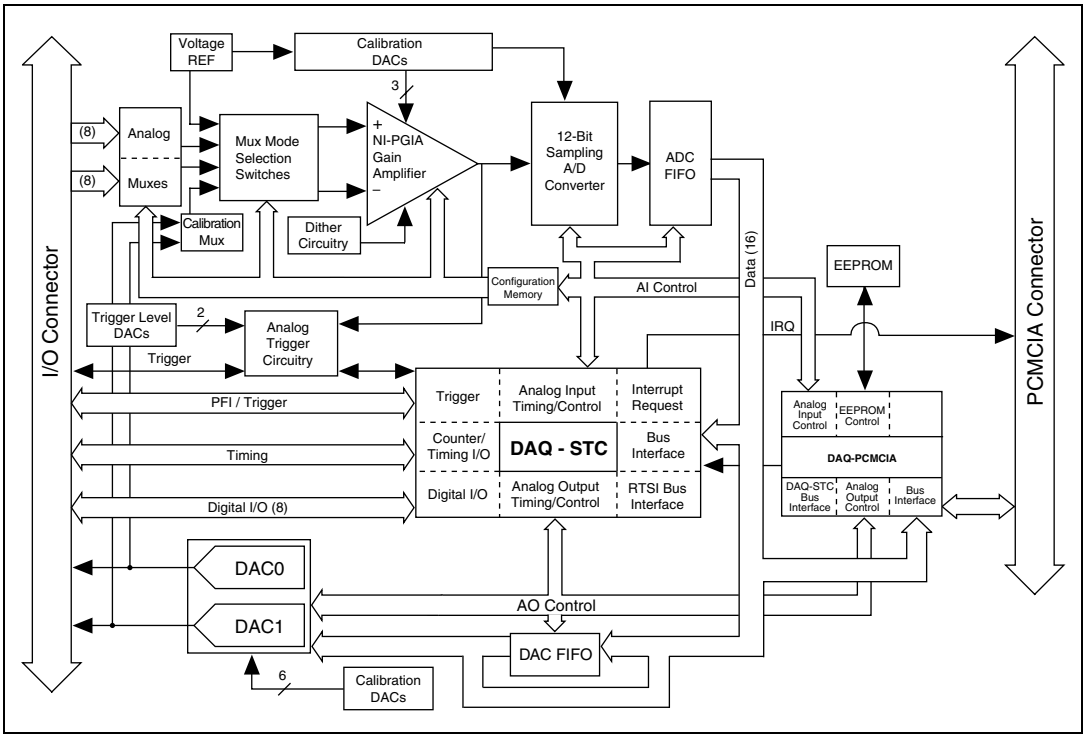


Figure 3-1. DAQCard-6062E Block Diagram

Analog Input

The analog input section of the DAQCard-6062E is software configurable. You can select different analog input configurations through application software designed to control the DAQCard-6062E. The following sections describe in detail each of the analog input categories.

Input Mode

The DAQCard-6062E has three different input modes: nonreferenced single-ended (NRSE) input, referenced single-ended (RSE) input, and differential (DIFF) input. The single-ended input configurations use up to 16 channels. The DIFF input configuration uses up to eight channels. Input modes are programmed on a per channel basis for multimode scanning. For example, you can configure the circuitry to scan 12 channels—four differentially configured channels and eight single-ended channels. Table 3-1 describes the three input configurations.

Table 3-1. Available Input Configurations for the DAQCard-6062E

Configuration	Description
DIFF	A channel configured in DIFF mode uses two analog channel input lines. One line connects to the positive input of the DAQCard-6062E programmable gain instrumentation amplifier (PGIA), and the other connects to the negative input of the PGIA.
RSE	A channel configured in RSE mode uses one analog channel input line, which connects to the positive input of the PGIA. The negative input of the PGIA is internally tied to analog input ground (AIGND).
NRSE	A channel configured in NRSE mode uses one analog channel input line, which connects to the positive input of the PGIA. The negative input of the PGIA connects to the analog input sense (AISENSE) input.

For more information about the three types of input configuration, refer to the *Analog Input Signal Connections* section of Chapter 4, *Signal Connections*, which contains diagrams showing the signal paths for the three configurations.

Input Polarity and Input Range

The DAQCard-6062E has two input polarities: unipolar and bipolar. Unipolar input means that the input voltage range is between 0 and V_{ref}, where V_{ref} is a positive reference voltage. Bipolar input means that the input voltage range is between $-V_{ref}/2$ and $+V_{ref}/2$. The DAQCard-6062E has a unipolar input range of 10 V (0 to 10 V) and a bipolar input range of 10 V (±5 V). You can program polarity and range settings on a per channel basis so that you can configure each input channel uniquely.

The software-programmable gain on these cards increases their overall flexibility by matching the input signal ranges to those that the ADC can accommodate. The DAQCard-6062E has gains of 0.5, 1, 2, 5, 10, 20, 50, and 100 and is suited for a wide variety of signal levels. With the proper gain setting, you can use the ADC's full resolution to measure the input signal. Table 3-2 shows the overall input range and precision according to the range configuration and gain used.

Table 3-2. Actual Range and Measurement Precision

Range Configuration	Gain	Actual Input Range	Resolution[1]
0 to +10 V	1.0	0 to +10 V	2.44 mV
	2.0	0 to +5 V	1.22 mV
	5.0	0 to +2 V	488.28 µV
	10.0	0 to +1 V	244.14 µV
	20.0	0 to +500 mV	122.07 µV
	50.0	0 to +200 mV	48.83 µV
	100.0	0 to +100 mV	24.41 µV
–5 to +5 V	0.5	–10 to +10 V	4.88 mV
	1.0	–5 to +5 V	2.44 mV
	2.0	–2.5 to +2.5 V	1.22 mV
	5.0	–1 to +1 V	488.28 µV
	10.0	–500 to +500 mV	244.14 µV
	20.0	–250 to +250 mV	122.07 µV
	50.0	–100 to +100 mV	48.83 µV
	100.0	–50 to +50 mV	24.41 µV

[1] The value of 1 LSB of the 12-bit ADC; that is, the voltage increment corresponding to a change of one count in the ADC 12-bit count.

Note: See Appendix A, *Specifications*, for absolute maximum ratings.

Considerations for Selecting Input Ranges

Which input polarity and range you select depends on the expected range of the incoming signal. A large input range can accommodate a large signal variation but reduces the voltage resolution. Choosing a smaller input range improves the voltage resolution but may result in the input signal going out of range. For best results, you should match the input range as closely as possible to the expected range of the input signal. For example, if you are certain the input signal will not be negative (below 0 V), unipolar input polarity is best. However, if the signal is negative or equal to zero, inaccurate readings will occur if you use unipolar input polarity.

Dither

When you enable dither, you add approximately 0.5 LSB rms of white Gaussian noise to the signal to be converted by the ADC. This addition is useful for applications involving averaging to increase the resolution of your DAQCard-6062E, as in calibration or spectral analysis. In such applications, noise modulation is decreased and differential linearity is improved by the addition of dither. When taking DC measurements, such as when checking the DAQCard-6062E calibration, you should enable dither and average about 1,000 points to take a single reading. This process removes the effects of quantization and reduces measurement noise, resulting in improved resolution. For high-speed applications not involving averaging or spectral analysis, you may want to disable the dither to reduce noise. You enable and disable the dither circuitry through software.

Figure 3-2 illustrates the effect of dither on signal acquisition. Figure 3-2a shows a small (±4 LSB) sine wave acquired with dither off. The quantization of the ADC is clearly visible. Figure 3-2b shows what happens when 50 such acquisitions are averaged together; quantization is still plainly visible. In Figure 3-2c, the sine wave is acquired with dither on. A considerable amount of noise is visible, but averaging about 50 such acquisitions, as shown in Figure 3-2d, eliminates both the added noise and the effects of quantization. Dither has the effect of forcing quantization noise to become a zero-mean random variable rather than a deterministic function of the input signal.

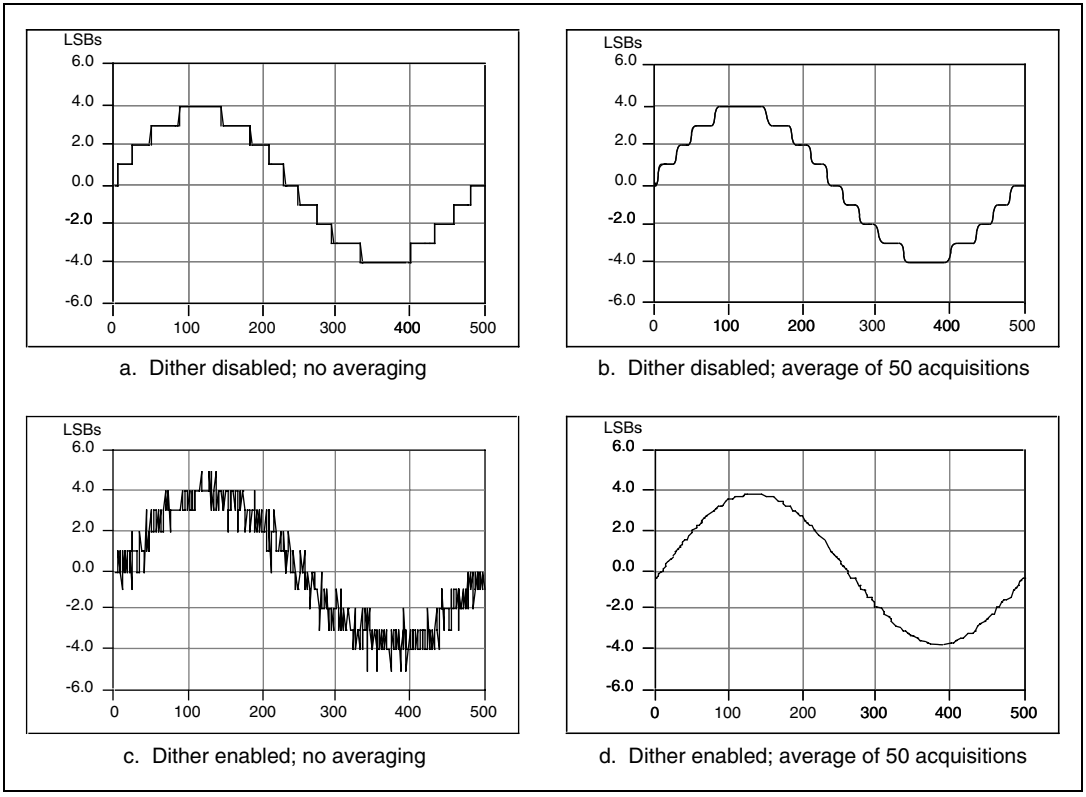


Figure 3-2. Dither

Multichannel Scanning Considerations

The DAQCard-6062E can scan multiple channels at the same maximum rate as their single-channel rate; however, pay careful attention to the settling times. No extra settling time is necessary between channels as long as the gain is constant and source impedances are low. Refer to Appendix A, *Specifications*, for a complete listing of settling times.

When scanning among channels at various gains, the settling times may increase. When the PGIA switches to a higher gain, the signal on the previous channel may be well outside the new, smaller range. For instance, suppose a 4 V signal is connected to channel 0 and a 1 mV signal is connected to channel 1, and suppose the PGIA is programmed to apply a gain of one to channel 0 and a gain of 100 to channel 1. When the multiplexer switches to channel 1 and the PGIA switches to a gain of 100, the new full-scale range is 100 mV (if the ADC is in unipolar mode).

The approximately 4 V step from 4 V to 1 mV is 4,000% of the new full-scale range. The circuitry may take as long as 100 µs to settle to 1 LSB after such a large transition. In general, this extra settling time is not needed when the PGIA is switching to a lower gain.

Settling times can also increase when scanning high-impedance signals due to a phenomenon called *charge injection*, where the analog input multiplexer injects a small amount of charge into each signal source when that source is selected. If the source impedance is not low enough, the effect of the charge—a voltage error—will not have decayed by the time the ADC samples the signal. For this reason, you should keep source impedances under 1 kΩ to perform high-speed scanning.

Due to the previously described limitations of settling times resulting from these conditions, multichannel scanning is not recommended unless sampling rates are low enough or it is necessary to sample several signals as nearly simultaneously as possible. The data is much more accurate and channel-to-channel independent if you acquire data from each channel independently (for example, 100 points from channel 0, then 100 points from channel 1, then 100 points from channel 2, and so on).

Analog Trigger

In addition to supporting internal software triggering and external digital triggering to initiate a data acquisition sequence, the DAQCard-6062E also supports analog triggering. You can configure the analog trigger circuitry to accept either a direct analog input from the PFI0/TRIG1 pin on the I/O connector or a postgain signal from the output of the PGIA, as shown in Figure 3-3. The trigger-level range for the direct analog channel is ±10 V in 78 mV steps. The range for the post-PGIA trigger selection is simply the full-scale range of the selected channel, and the resolution is that range divided by 256.

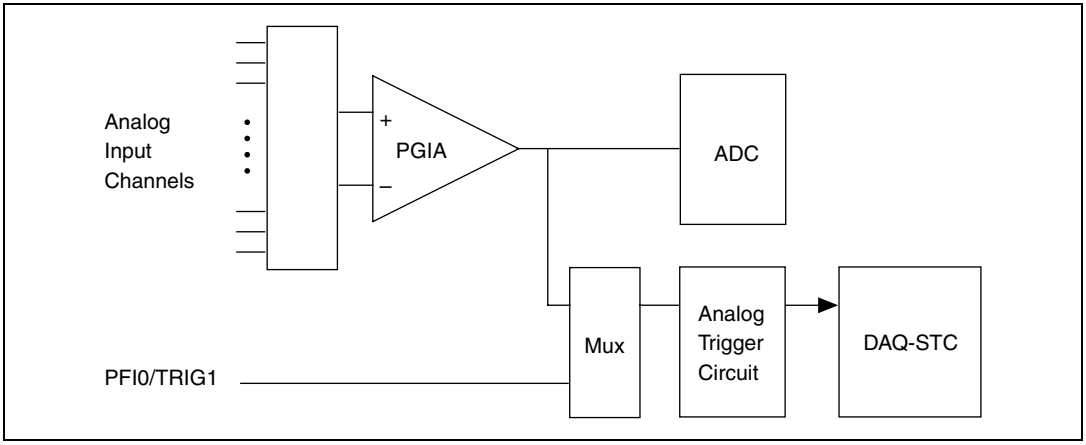


Figure 3-3. Analog Trigger Block Diagram

Five analog triggering modes are available, as shown in Figures 3-4 through 3-8. You can set **lowValue** and **highValue** independently in software.

In below-low-level analog triggering mode, as shown in Figure 3-4, the trigger is generated when the signal value is less than **lowValue**. **HighValue** is unused.

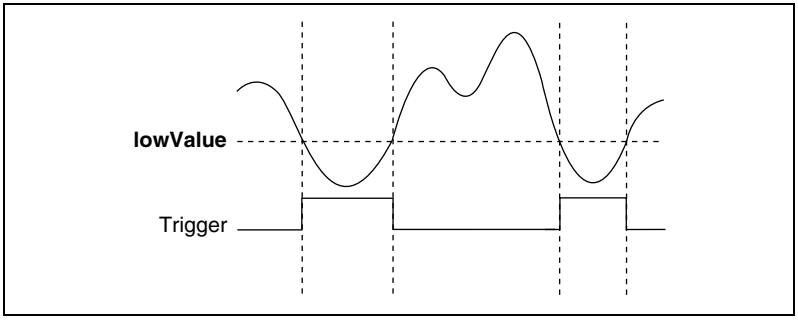


Figure 3-4. Below-Low-Level Analog Triggering Mode

In above-high-level analog triggering mode, as shown in Figure 3-5, the trigger is generated when the signal value is greater than **highValue**. **LowValue** is unused.

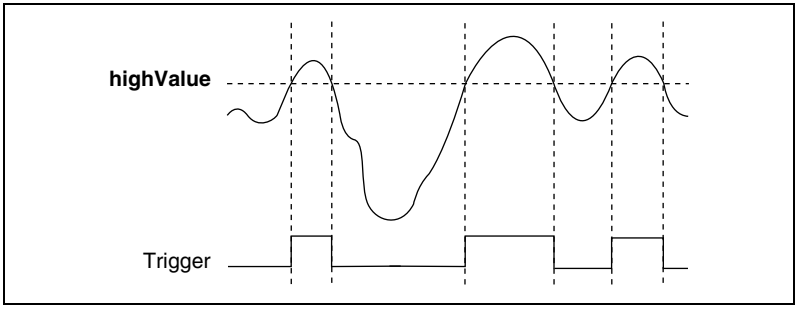


Figure 3-5. Above-High-Level Analog Triggering Mode

In inside-region analog triggering mode, as shown in Figure 3-6, the trigger is generated when the signal value is between the **lowValue** and the **highValue.**

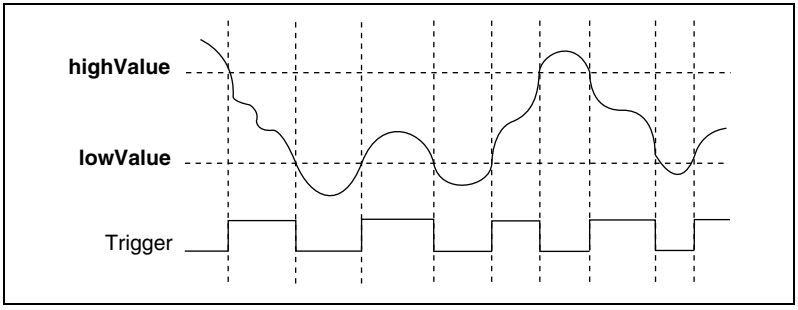


Figure 3-6. Inside-Region Analog Triggering Mode

In high-hysteresis analog triggering mode, as shown in Figure 3-7, the trigger is generated when the signal value is greater than **highValue**, with the hysteresis specified by **lowValue.**

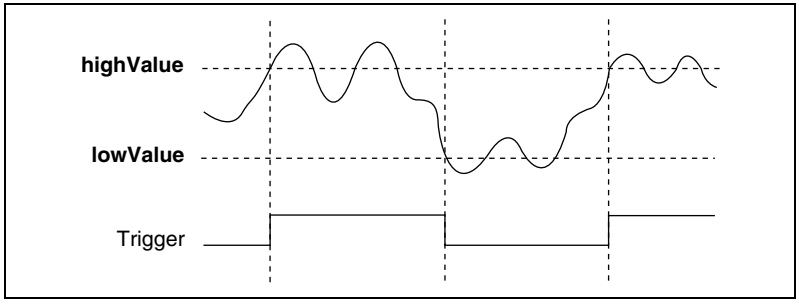


Figure 3-7. High-Hysteresis Analog Triggering Mode

In low-hysteresis analog triggering mode, as shown in Figure 3-8, the trigger is generated when the signal value is less than **lowValue**, with the hysteresis specified by **highValue.**

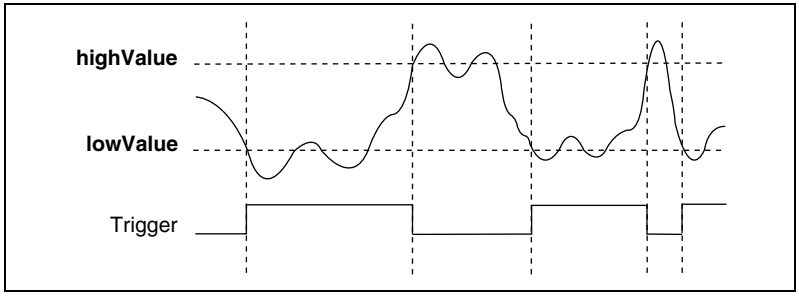


Figure 3-8. Low-Hysteresis Analog Triggering Mode

The analog trigger circuit generates an internal digital trigger based on the analog input signal and the user-defined trigger levels. This digital trigger can be used by any of the timing sections of the DAQ-STC, including the analog input, analog output, and general-purpose counter/timer sections. For example, the analog input section can be configured to acquire *n* scans after the analog input signal crosses a specific threshold. As another example, the analog output section can be configured to update its outputs whenever the analog input signal crosses a specific threshold.

Digital I/O

The DAQCard-6062E contains eight lines of digital I/O for general-purpose use. You can individually configure each line through software for either input or output. At system startup and reset, the digital I/O ports are all high impedance.

The hardware up/down control for general-purpose counters 0 and 1 are connected onboard to DIO6 and DIO7, respectively. Thus, you can use DIO6 and DIO7 to control the general-purpose counters. The up/down control signals are input only and do not affect the operation of the DIO lines.

Timing Signal Routing

The DAQ-STC provides a very flexible interface for connecting timing signals to other boards or external circuitry. Your DAQCard-6062E uses the Programmable Function Input (PFI) pins on the I/O connector to connect to external circuitry. These connections are designed to enable the DAQCard-6062E to both control and be controlled by other boards and circuits.

The DAQ-STC has a total of 13 internal timing signals that can be controlled by an external source. These timing signals can also be controlled by signals generated internally to the DAQ-STC, and these selections are fully software configurable. For example, the signal routing multiplexer for controlling the CONVERT* signal is shown in Figure 3-9.

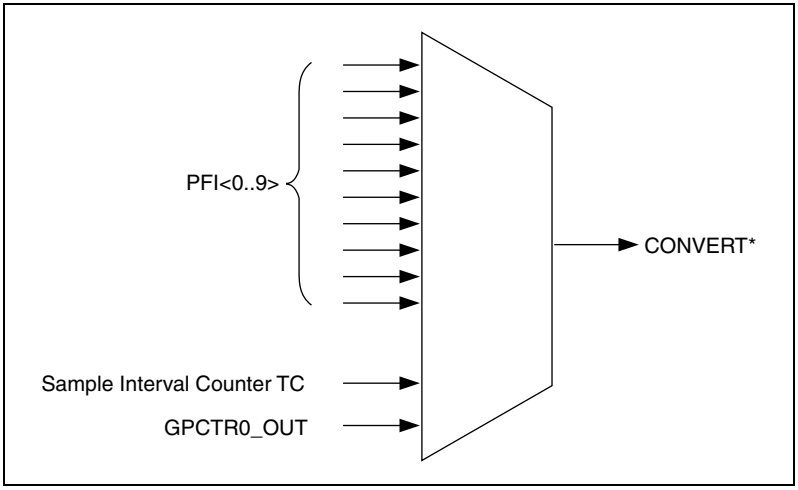


Figure 3-9. CONVERT* Signal Routing

This figure shows that CONVERT* can be generated from a number of sources, including the external signals PFI<0..9> and the internal signals Sample Interval Counter TC and GPCTR0_OUT.

Programmable Function Inputs

The 10 PFIs are connected to the signal routing multiplexer for each timing signal, and software can select one of the PFIs as the external source for a given timing signal. It is important to note that any of the PFIs can be used as an input by any of the timing signals and that multiple timing signals can use the same PFI simultaneously. This flexible routing scheme reduces the need to change physical connections to the I/O connector for different applications.

You can also individually enable each of the PFI pins to output a specific internal timing signal. For example, if you need the UPDATE* signal as an output on the I/O connector, software can turn on the output driver for the PFI5/UPDATE* pin.

DAQCard-6062E Clocks

Many functions performed by the DAQCard-6062E require a frequency timebase to generate the necessary timing signals for controlling A/D conversions, DAC updates, or general-purpose signals at the I/O connector.

The DAQCard-60602E can directly use its internal 20 MHz timebase as the primary frequency source.

4

Signal Connections

This chapter describes how to make input and output signal connections to your DAQCard-6062E through the DAQCard I/O connector.

The I/O connector for the DAQCard-6062E has 68 pins that you can connect to 68-pin accessories with the SHC68-68EP shielded cable. You can connect your DAQCard-6062E to 50-pin signal accessories using the SHC68-68-EP cable in conjunction with the 68M-50F adapter.

I/O Connector

Figure 4-1 shows the pin assignments for the 68-pin I/O connector on the DAQCard-6062E. A signal description follows the connector pinout.

Warning Exceeding the differential and common-mode input ranges distorts your input signals. Exceeding the maximum input voltage rating can damage the DAQCard-6062E and your computer. National Instruments is *not* liable for any damages resulting from such signal connections. The maximum input voltage ratings are listed in Table 4-2 in the *Protection* column.

ACH8	34	68	ACH0
ACH1	33	67	AIGND
AIGND	32	66	ACH9
ACH10	31	65	ACH2
ACH3	30	64	AIGND
AIGND	29	63	ACH11
ACH4	28	62	AISENSE
AIGND	27	61	ACH12
ACH13	26	60	ACH5
ACH6	25	59	AIGND
AIGND	24	58	ACH14
ACH15	23	57	ACH7
DAC0OUT	22	56	AIGND
DAC1OUT	21	55	AOGND
EXTREF	20	54	AOGND
DIO4	19	53	DGND
DGND	18	52	DIO0
DIO1	17	51	DIO5
DIO6	16	50	DGND
DGND	15	49	DIO2
+5 V	14	48	DIO7
DGND	13	47	DIO3
DGND	12	46	SCANCLK
PFI0/TRIG1	11	45	EXTSTROBE*
PFI1/TRIG2	10	44	DGND
DGND	9	43	PFI2/CONVERT*
+5 V	8	42	PFI3/GPCTR1_SOURCE
DGND	7	41	PFI4/GPCTR1_GATE
PFI5/UPDATE*	6	40	GPCTR1_OUT
PFI6/WFTRIG	5	39	DGND
DGND	4	38	PFI7/STARTSCAN
PFI9/GPCTR0_GATE	3	37	PFI8/GPCTR0_SOURCE
GPCTR0_OUT	2	36	DGND
FREQ_OUT	1	35	DGND

Figure 4-1. I/O Connector Pin Assignment for the DAQCard-6062E

Table 4-1 describes the DAQCard-6062E I/O connectors as diagrammed in Figure 4-1.

Table 4-1. I/O Connector Signal Descriptions

Signal Name	Reference	Direction	Description
AIGND	—	—	Analog Input Ground—These pins are the reference point for single-ended measurements and the bias current return point for differential measurements. All three ground references—AIGND, AOGND, and DGND—are connected together on your DAQCard-6062E card.
ACH<0..15>	AIGND	Input	Analog Input Channels 0 through 15—Each channel pair, ACH<*i*, *i*+8> (*i* = 0..7), can be configured as either one differential input or two single-ended inputs.
AISENSE	AIGND	Input	Analog Input Sense—This pin serves as the reference node for any of channels ACH<0..15> in NRSE configuration.
DAC0OUT	AOGND	Output	Analog Channel 0 Output—This pin supplies the voltage output of analog output channel 0.
DAC1OUT	AOGND	Output	Analog Channel 1 Output—This pin supplies the voltage output of analog output channel 1.
AOGND	—	—	Analog Output Ground—This node references the analog output voltages. All three ground references—AIGND, AOGND, and DGND—are connected together on your DAQCard-6062E card.
DGND	—	—	Digital Ground—This pin supplies the reference for the digital signals at the I/O connector as well as the +5 VDC supply. All three ground references—AIGND, AOGND, and DGND—are connected together on your DAQCard-6062E.
DIO<0..7>	DGND	Input or Output	Digital I/O signals—DIO6 and DIO7 can control the up/down signal of general-purpose counters 0 and 1, respectively.
+5 V	DGND	Output	+5 VDC Source—These pins are fused for up to 250 mA of +5 V supply. The fuse is self-resetting.
SCANCLK	DGND	Output	Scan Clock—This pin pulses once for each A/D conversion in the scanning modes when enabled. The low-to-high edge indicates when the input signal can be removed from the input or switched to another signal.
EXTSTROBE*	DGND	Output	External Strobe—This output can be toggled under software control to latch signals or trigger events on external devices.

Table 4-1. I/O Connector Signal Descriptions (Continued)

Signal Name	Reference	Direction	Description
PFI0/TRIG1	DGND	Input Output	PFI0/Trigger 1—As an input, this is either one of the PFIs or the source for the hardware analog trigger. PFI signals are explained in the *Timing Connections* section later in this chapter. The hardware analog trigger is explained in the *Analog Trigger* section of Chapter 3, *Hardware Overview*. As an output, this is the TRIG1 (AI Start Trigger) signal. In posttrigger data acquisition sequences, a low-to-high transition indicates the initiation of the acquisition sequence. In pretrigger applications, a low-to-high transition indicates the initiation of the pretrigger conversions.
PFI1/TRIG2	DGND	Input Output	PFI1/Trigger 2—As an input, this is one of the PFIs. As an output, this is the TRIG2 (AI Stop Trigger) signal. In pretrigger applications, a low-to-high transition indicates the initiation of the posttrigger conversions. TRIG2 is not used in posttrigger applications.
PFI2/CONVERT*	DGND	Input Output	PFI2/Convert—As an input, this is one of the PFIs. As an output, this is the CONVERT* (AI Convert) signal. A high-to-low edge on CONVERT* indicates that an A/D conversion is occurring.
PFI3/GPCTR1_SOURCE	DGND	Input Output	PFI3/Counter 1 Source—As an input, this is one of the PFIs. As an output, this is the GPCTR1_SOURCE signal. This signal reflects the actual source connected to general-purpose counter 1.
PFI4/GPCTR1_GATE	DGND	Input Output	PFI4/Counter 1 Gate—As an input, this is one of the PFIs. As an output, this is the GPCTR1_GATE signal. This signal reflects the actual gate signal connected to general-purpose counter 1.
GPCTR1_OUT	DGND	Output	Counter 1 Output—This output is from the general-purpose counter 1 output.
PFI5/UPDATE*	DGND	Input Output	PFI5/Update—As an input, this is one of the PFIs. As an output, this is the UPDATE* (AO Update) signal. A high-to-low edge on UPDATE* indicates that the analog output primary group is being updated.

Table 4-1. I/O Connector Signal Descriptions (Continued)

Signal Name	Reference	Direction	Description
PFI6/WFTRIG	DGND	Input	PFI6/Waveform Trigger—As an input, this is one of the PFIs.
		Output	As an output, this is the WFTRIG (AO Start Trigger) signal. In timed analog output sequences, a low-to-high transition indicates the initiation of the waveform generation.
PFI7/STARTSCAN	DGND	Input	PFI7/Start of Scan—As an input, this is one of the PFIs.
		Output	As an output, this is the STARTSCAN (AI Scan Start) signal. This pin pulses once at the start of each analog input scan in the interval scan. A low-to-high transition indicates the start of the scan.
PFI8/GPCTR0_SOURCE	DGND	Input	PFI8/Counter 0 Source—As an input, this is one of the PFIs.
		Output	As an output, this is the GPCTR0_SOURCE signal. This signal reflects the actual source connected to general-purpose counter 0.
PFI9/GPCTR0_GATE	DGND	Input	PFI9/Counter 0 Gate—As an input, this is one of the PFIs.
		Output	As an output, this is the GPCTR0_GATE signal. This signal reflects the actual gate signal connected to general-purpose counter 0.
GPCTR0_OUT	DGND	Output	Counter 0 Output—This output is from the general-purpose counter 0 output.
FREQ_OUT	DGND	Output	Frequency Output—This output is from the frequency generator output.

Table 4-2 shows the I/O signal summary for the DAQCard-6062E.

Table 4-2. I/O Signal Summary, DAQCard-6062E

Signal Name	Drive	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
ACH<0..15>	AI	100 GΩ in parallel with 100 pF	25/10	—	—	—	±200 pA
AISENSE	AI	100 GΩ in parallel with 100 pF	25/10	—	—	—	±200 pA
AIGND	AI	—	—	—	—	—	—
DAC0OUT	AO	0.1 Ω	Short-circuit to ground	5 at 10	5 at –10	10 V/µs	—
DAC1OUT	AO	0.1 Ω	Short-circuit to ground	5 at 10	5 at –10	10 V/µs	—
AOGND	—	—	—	—	—	—	—
DGND	DO	—	—	—	—	—	—
VCC	DO	0.45 Ω	Short-circuit to ground	250 at V_{cc}	—	—	—
DIO<0..7>	DIO	—	V_{cc} +0.5	13 at (V_{cc} –0.4)	24 at 0.4	1.1	50 kΩ pu[1]
SCANCLK	DO	—	—	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
EXTSTROBE*	DO	—	—	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI0/TRIG1	ADIO	10 kΩ	V_{cc} +0.5/±35	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu[2]
PFI1/TRIG2	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI2/CONVERT*	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI3/GPCTR1_SOURCE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI4/GPCTR1_GATE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu

Table 4-2. I/O Signal Summary, DAQCard-6062E (Continued)

Signal Name	Drive	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
GPCTR1_OUT	DO	—	—	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI5/UPDATE*	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI6/WFTRIG	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI7/STARTSCAN	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI8/GPCTR0_SOURCE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI9/GPCTR0_GATE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
GPCTR0_OUT	DO	—	—	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
FREQ_OUT	DO	—	—	3.5 at (V_{cc}–0.4)	5 at 0.4	1.5	50 kΩ pu

AI = Analog Input DIO = Digital Input/Output pu = pullup
DO = Digital Output ADIO = Analog/Digital Input/Output AO = Analog Output

[1] DIO <6..7> are also pulled up with a 10 kΩ resistor.

[2] Also pulled down with a 10 kΩ resistor.

Note: The tolerance on the 50 kΩ pullup and pulldown resistors is very large. Actual values may range between 17 kΩ and 100 kΩ.

Warning: Unless specifically indicated in the Protection column of Table 4-2, the outputs of DAQCard-6062E cards are not short-circuit protected. Exceeding the output limit in the Source and Sink columns can damage your DAQCard-6062E.

Analog Input Signal Connections

The analog input signals are ACH<0..15>, AISENSE, and AIGND. The ACH<0..15> signals are tied to the 16 analog input channels of your DAQCard-6062E. In single-ended mode, signals connected to ACH<0..15> are routed to the positive input of the DAQCard PGIA. In differential mode, signals connected to ACH<0..7> are routed to the positive input of the PGIA, and signals connected to ACH<8..15> are routed to the negative input of the PGIA.

Warning Exceeding the differential and common-mode input ranges distorts your input signals[1]. Exceeding the maximum input voltage rating can damage the DAQCard-6062E and your computer. National Instruments is *not* liable for any damages resulting from such signal connections. The maximum input voltage ratings are listed in Table 4-2 in the *Protection* column.

In NRSE mode, the AISENSE signal is connected internally to the negative input of the DAQCard PGIA when their corresponding channels are selected. In DIFF and RSE modes, this signal is left unconnected.

AIGND is an analog input common signal that is routed directly to the ground tie point on the DAQCards. You can use this signal for a general analog ground tie point to your DAQCard-6062E, if necessary.

Connection of analog input signals to your DAQCard-6062E depends on the configuration of the analog input channels you are using and the type of input signal source. With the different configurations, you can use the PGIA in different ways. Figure 4-2 shows a diagram of your DAQCard PGIA.

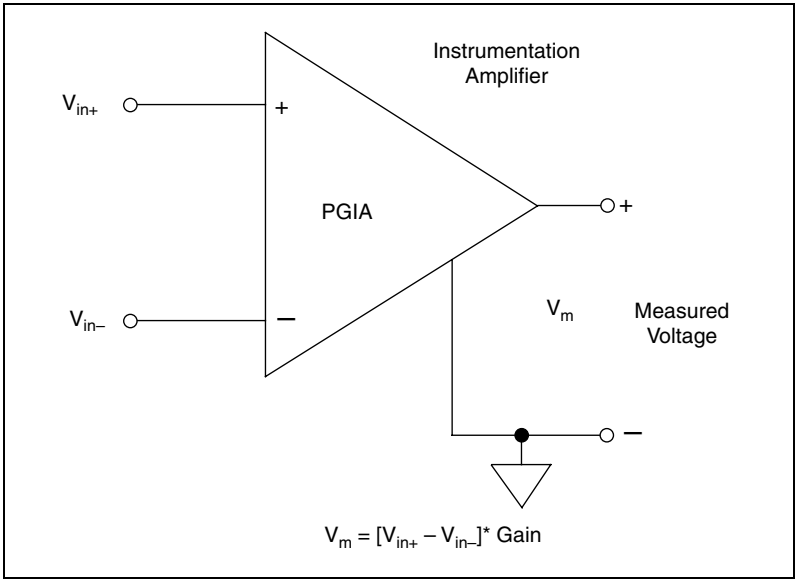


Figure 4-2. DAQCard-6062E PGIA

[1] Note that exceeding input ranges on any channel can affect the measurements on a different channel even if the other channel is well within the input range.

The PGIA applies gain and common-mode voltage rejection and presents high input impedance to the analog input signals connected to your DAQCard-6062E. Signals are routed to the positive and negative inputs of the PGIA through input multiplexers on the DAQCard-6062E. The PGIA converts two input signals to a signal that is the difference between the two input signals multiplied by the gain setting of the amplifier. The amplifier output voltage is referenced to the ground for the DAQCard-6062E. Your DAQCard-6062E ADC measures this output voltage when it performs A/D conversions.

You must reference all signals to ground either at the source device or at the DAQCard-6062E. If you have a floating source, you should reference the signal to ground by using the RSE input mode or the DIFF input configuration with bias resistors (see the *Differential Connections for Nonreferenced or Floating Signal Sources* section). If you have a grounded source, you should not reference the signal to AIGND. You can avoid this reference by using DIFF or NRSE input configurations.

Types of Signal Sources

When configuring the input channels and making signal connections, you must first determine whether the signal sources are floating or ground-referenced. The following sections describe these two types of signals.

Floating Signal Sources

A floating signal source is one that is not connected in any way to the building ground system but, rather, has an isolated ground-reference point. Some examples of floating signal sources are outputs of transformers, thermocouples, battery-powered devices, optical isolator output, and isolation amplifiers. An instrument or device that has an isolated output is a floating signal source. You must tie the ground reference of a floating signal to your DAQCard-6062E analog input ground to establish a local or onboard reference for the signal. Otherwise, the measured input signal varies as the source floats out of the common-mode input range.

Ground-Referenced Signal Sources

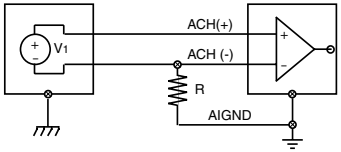
A ground-referenced signal source is one that is connected in some way to the building system ground and is, therefore, already connected to a common ground point with respect to the DAQCard-6062E, assuming that the computer is plugged into the same power system. Non-isolated output of instruments and devices that plug into the building power system falls into this category.

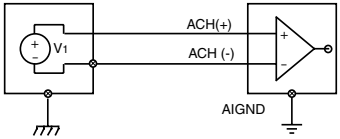
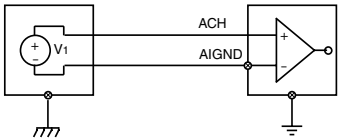
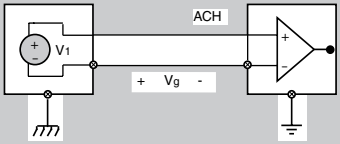
The difference in ground potential between two instruments connected to the same building power system is typically between 1 and 100 mV, but it can be much higher if power distribution circuits are not properly connected. If a grounded signal source is improperly measured, this difference may appear as an error in the measurement. The connection instructions for grounded signal sources are designed to eliminate this ground potential difference from the measured signal.

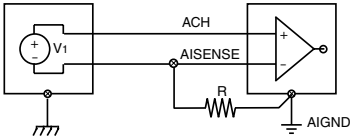
Input Configurations

You can configure your DAQCard-6062E for one of three input modes: NRSE, RSE, or DIFF. The following sections discuss the use of single-ended and differential measurements and considerations for measuring both floating and ground-referenced signal sources.

Figure 4-3 summarizes the recommended input configuration for both types of signal sources.

<table>
<tr><td rowspan="2"></td><td colspan="2">Signal Source Type</td></tr>
<tr><td>Floating Signal Source
(Not Connected to Building Ground)</td><td>Grounded Signal Source</td></tr>
<tr><td>Input</td><td>Examples
• Ungrounded Thermocouples
• Signal conditioning with isolated outputs
• Battery devices</td><td>Examples
• Plug-in instruments with nonisolated outputs</td></tr>
<tr><td>Differential
(DIFF)</td><td> 

See text for information on bias resistors.</td><td> 
</td></tr>
<tr><td>Single-Ended —
Ground
Referenced
(RSE)</td><td> 
</td><td>NOT RECOMMENDED
 

Ground-loop losses, Vg, are added to measured signal</td></tr>
<tr><td>Single-Ended —
Nonreferenced
(NRSE)</td><td> 

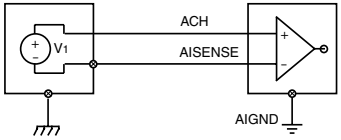
See text for information on bias resistors.</td><td> 
</td></tr>
</table>

Figure 4-3. Summary of Analog Input Connections

Differential Connection Considerations (DIFF Input Configuration)

A differential connection is one in which the DAQCard-6062E analog input signal has its own reference signal or signal return path. These connections are available when the selected channel is configured in DIFF input mode. The input signal is tied to the positive input of the PGIA, and its reference signal, or return, is tied to the negative input of the PGIA.

When you configure a channel for differential input, each signal uses two multiplexer inputs—one for the signal and one for its reference signal. Therefore, with a differential configuration for every channel, up to eight analog input channels are available.

You should use differential input connections for any channel that meets any of the following conditions:

- The input signal is low level (less than 1 V).
- The leads connecting the signal to the DAQCard-6062E are greater than 10 ft (3 m).
- The input signal requires a separate ground-reference point or return signal.
- The signal leads travel through noisy environments.

Differential signal connections reduce picked-up noise and increase common-mode noise rejection. Differential signal connections also allow input signals to float within the common-mode limits of the PGIA.

Differential Connections for Ground-Referenced Signal Sources

Figure 4-4 shows how to connect a ground-referenced signal source to a channel on a DAQCard-6062E configured in DIFF input mode.

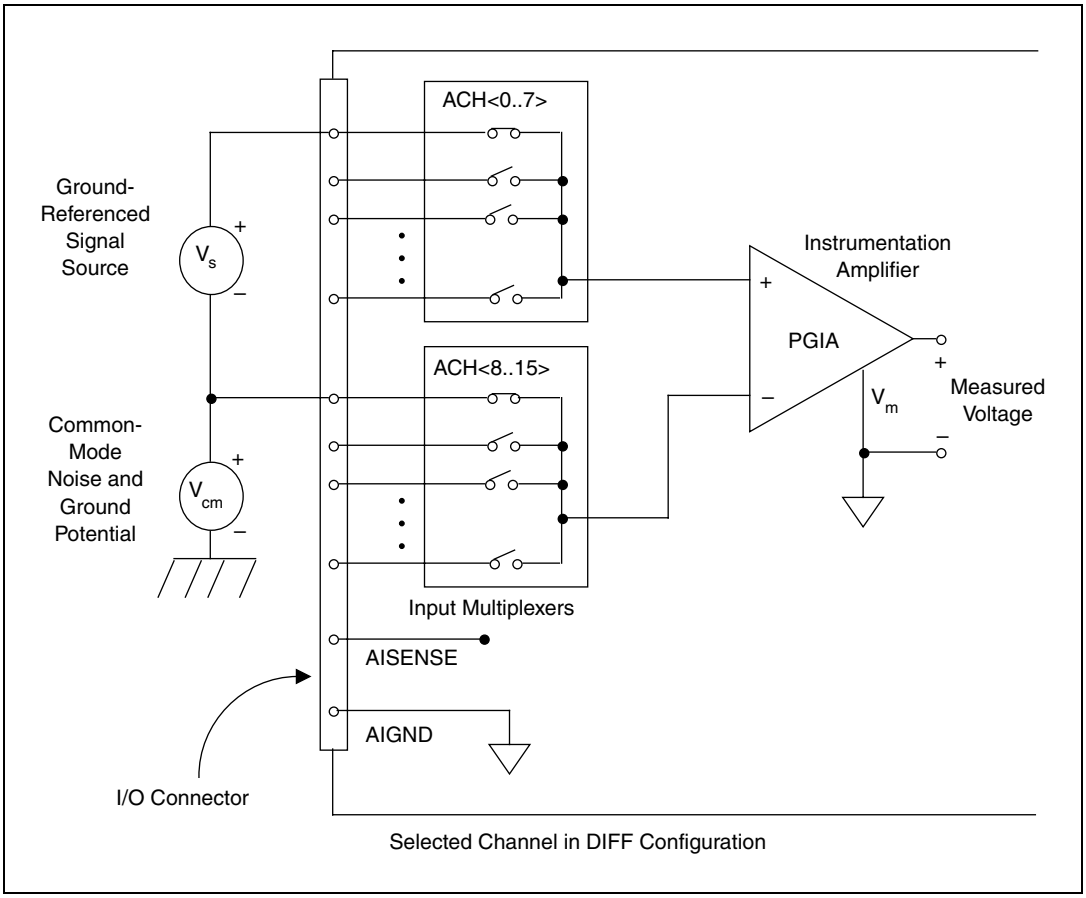


Figure 4-4. Differential Input Connections for Ground-Referenced Signals

With this type of connection, the PGIA rejects both the common-mode noise in the signal and the ground potential difference between the signal source and the DAQCard-6062E ground, shown as V_{cm} in Figure 4-4.

Differential Connections for Nonreferenced or Floating Signal Sources

Figure 4-5 shows how to connect a floating signal source to a channel on a DAQCard-6062E configured in DIFF input mode.

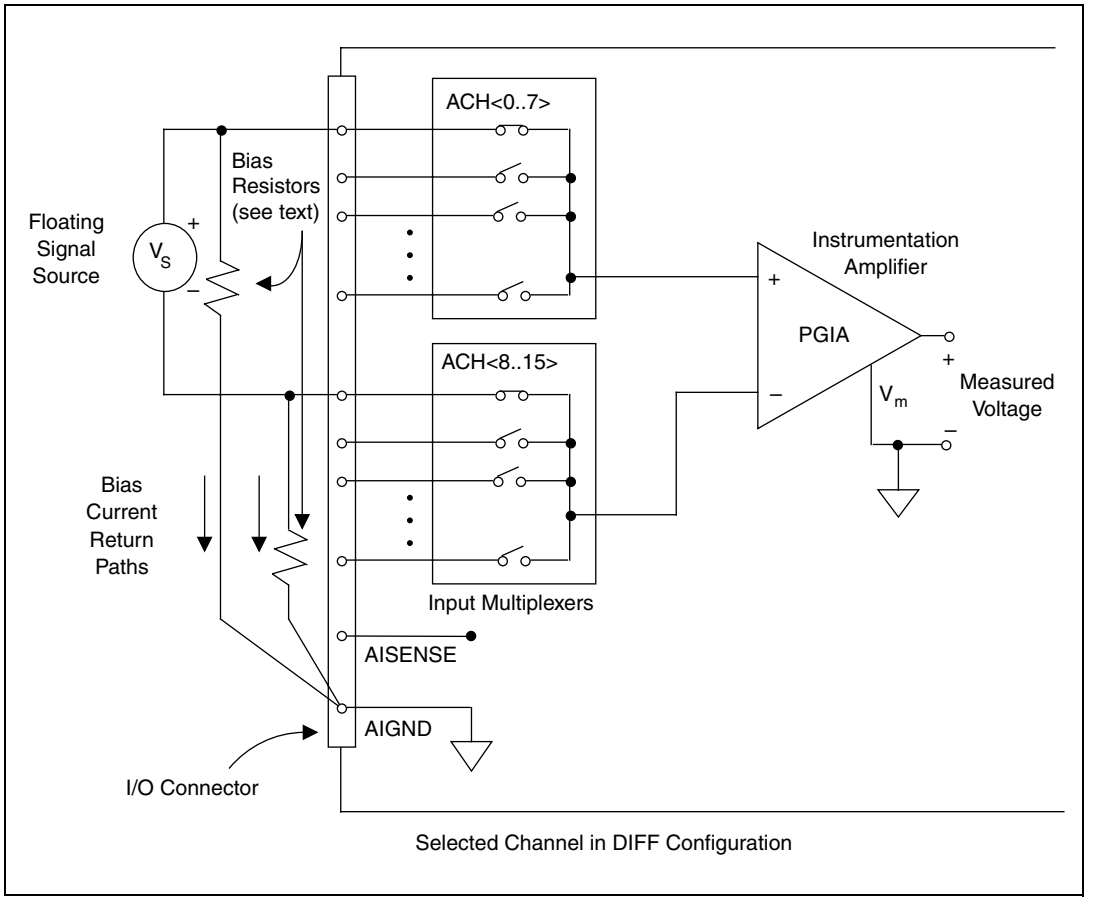


Figure 4-5. Differential Input Connections for Nonreferenced Signals

Figure 4-5 shows two bias resistors connected in parallel with the signal leads of a floating signal source. If you do not use the resistors and the source is truly floating, the source is not likely to remain within the common-mode signal range of the PGIA, and the PGIA will saturate, causing erroneous readings. You must reference the source to AIGND. The easiest way is to connect the positive side of the signal to the positive input of the PGIA and connect the negative side of the signal to AIGND as well as to the negative input of the PGIA, without any resistors at all.

This connection works well for DC-coupled sources with low source impedance (less than 100 Ω).

However, for larger source impedances, this connection leaves the differential signal path significantly out of balance. Noise that couples electrostatically onto the positive line does not couple onto the negative line because it is connected to ground. Hence, this noise appears as a differential-mode signal instead of a common-mode signal, so the PGIA does not reject it. In this case, instead of directly connecting the negative line to AIGND, connect it to AIGND through a resistor that is about 100 times the equivalent source impedance. The resistor puts the signal path nearly in balance, so that about the same amount of noise couples onto both connections, yielding better rejection of electrostatically coupled noise. Also, this configuration does not load down the source (other than the very high input impedance of the PGIA).

You can fully balance the signal path by connecting another resistor of the same value between the positive input and AIGND, as shown in Figure 4-5. This fully-balanced configuration offers slightly better noise rejection but has the disadvantage of loading the source down with the series combination (sum) of the two resistors. If, for example, the source impedance is 2 kΩ and each of the two resistors is 100 kΩ, the resistors load down the source with 200 kΩ and produce a –1% gain error.

Both inputs of the PGIA require a DC path to ground in order for the PGIA to work. If the source is AC coupled (capacitively coupled), the PGIA needs a resistor between the positive input and AIGND. If the source has low impedance, choose a resistor that is large enough not to significantly load the source but small enough not to produce significant input offset voltage as a result of input bias current (typically 100 kΩ to 1 MΩ). In this case, you can tie the negative input directly to AIGND. If the source has high output impedance, balance the signal path as previously described using the same value resistor on both the positive and negative inputs; be aware that there is some gain error from loading down the source.

Single-Ended Connection Considerations

A single-ended connection is one in which the DAQCard-6062E analog input signal is referenced to a ground that can be shared with other input signals. The input signal is tied to the positive input of the PGIA, and the ground is tied to the negative input of the PGIA.

When every channel is configured for single-ended input, up to 16 analog input channels are available.

Use single-ended input connections for any input signal that meets the following conditions:

- The input signal is high level (greater than 1 V).
- The leads connecting the signal to the DAQCard-6062E are less than 10 ft (3 m).
- The input signal can share a common reference point with other signals.

DIFF input connections are recommended for greater signal integrity for any input signal that does not meet the preceding conditions.

You can software-configure the DAQCard-6062E channels for two different types of single-ended connections—RSE configuration and NRSE configuration. Use the RSE configuration for floating signal sources; in this case, the DAQCard-6062E provides the reference ground point for the external signal. Use the NRSE input configuration for ground-referenced signal sources; in this case, the external signal supplies its own reference ground point and the DAQCard-6062E should not supply one.

In single-ended configurations, more electrostatic and magnetic noise couples into the signal connections than in differential configurations. The coupling is the result of differences in the signal path. Magnetic coupling is proportional to the area between the two signal conductors. Electrical coupling is a function of how much the electric field differs between the two conductors.

Single-Ended Connections for Floating Signal Sources (RSE Configuration)

Figure 4-6 shows how to connect a floating signal source to a channel on a DAQCard-6062E configured for RSE mode.

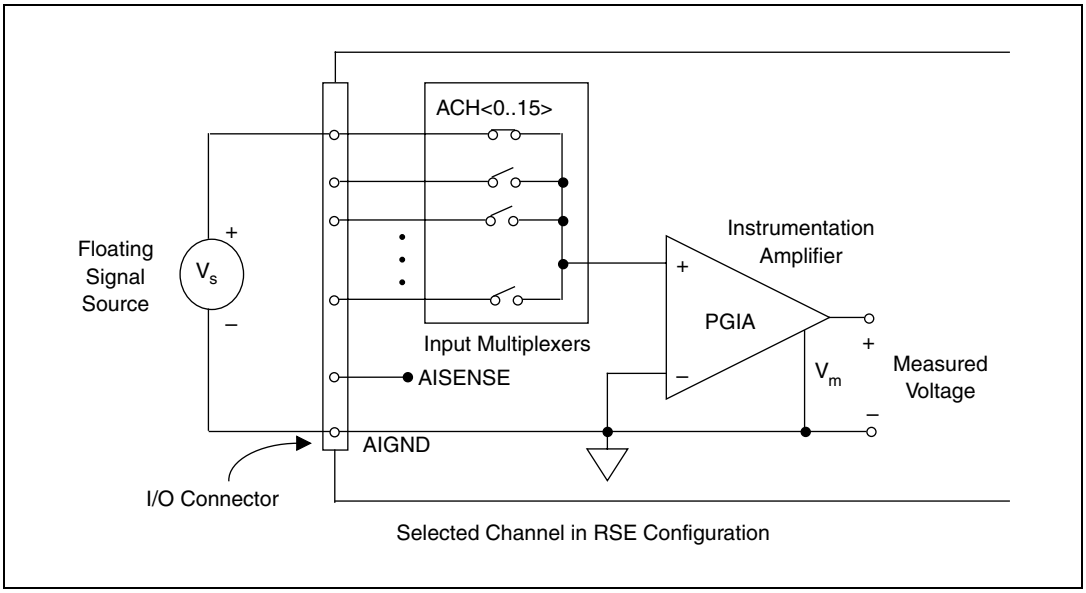


Figure 4-6. Single-Ended Input Connections for Nonreferenced or Floating Signals

Single-Ended Connections for Grounded Signal Sources (NRSE Configuration)

To measure a grounded signal source with a single-ended configuration, you must configure your DAQCard-6062E in the NRSE input configuration. The signal is then connected to the positive input of the DAQCard PGIA, and the signal local ground reference is connected to the negative input of the PGIA. The ground point of the signal should, therefore, be connected to the AISENSE pin. Any potential difference between the DAQCard-6062E ground and the signal ground appears as a common-mode signal at both the positive and negative inputs of the PGIA, and this difference is rejected by the amplifier. If the input circuitry of a DAQCard-6062E were referenced to ground, in this situation as in the RSE input configuration, this difference in ground potentials would appear as an error in the measured voltage.

Figure 4-7 shows how to connect a grounded signal source to a channel on a DAQCard-6062E configured for NRSE mode.

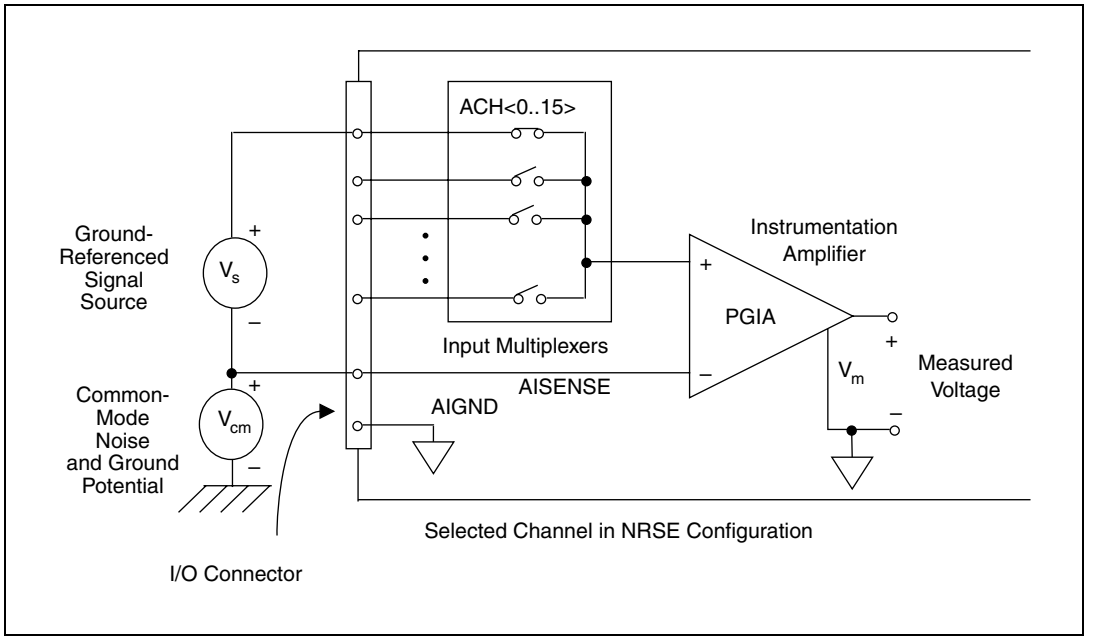


Figure 4-7. Single-Ended Input Connections for Ground-Referenced Signals

Common-Mode Signal Rejection Considerations

Figures 4-4 and 4-7 show connections for signal sources that are already referenced to some ground point with respect to the DAQCard-6062E. In these cases, the PGIA can reject any voltage caused by ground potential differences between the signal source and the DAQCard-6062E.
In addition, with differential input connections, the PGIA can reject common-mode noise pickup in the leads connecting the signal sources to the DAQCard-6062E. The PGIA can reject common-mode signals as long as V^+_{in} and V^-_{in} are both within ±11 V of AIGND.

Analog Output Signal Connections

The analog output signals are DAC0OUT, DAC1OUT, EXTREF, and AOGND.

- DAC0OUT is the voltage output signal for analog output channel 0.
- DAC1OUT is the voltage output signal for analog output channel 1.

EXTREF is the external reference input for both analog output channels. You must configure each analog output channel individually for external reference selection in order for the signal applied at the external reference input to be used by that channel. If you do not specify an external reference, the channel will use the internal reference. Analog output configuration options are explained in the *Analog Input* section of Chapter 3, *Hardware Overview*. The following ranges and ratings apply to the EXTREF input:

- Usable input voltage range: ±11 V peak with respect to AOGND
- Absolute maximum ratings: ±15 V peak with respect to AOGND

AOGND is the ground reference signal for both analog output channels and the external reference signal.

Figure 4-8 shows how to make analog output connections and the external reference input connection to your DAQCard-6062E.

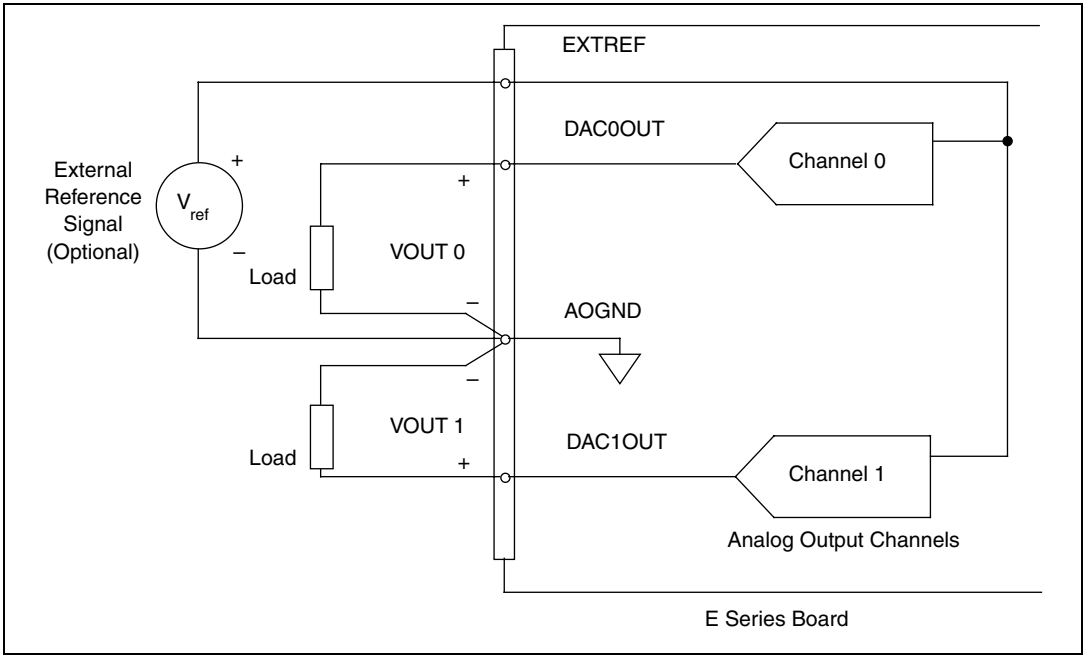


Figure 4-8. Analog Output Connections

The external reference signal can be either a DC signal or an AC signal. The board multiplies this reference signal by the DAC code (divided by the full-scale DAC code) to generate the output voltage.

Digital I/O Signal Connections

The digital I/O signals are DIO<0..7> and DGND. The DIO<0..7> signals make up the DIO port, and DGND is the ground reference signal for this port. You can program all lines individually to be inputs or outputs.

Warning Exceeding the maximum input voltage ratings, which are listed in Table 4-2, can damage the DAQCard-6062E and the computer. National Instruments is *not* liable for any damages resulting from such signal connections.

Figure 4-9 shows signal connections for three typical digital I/O applications.

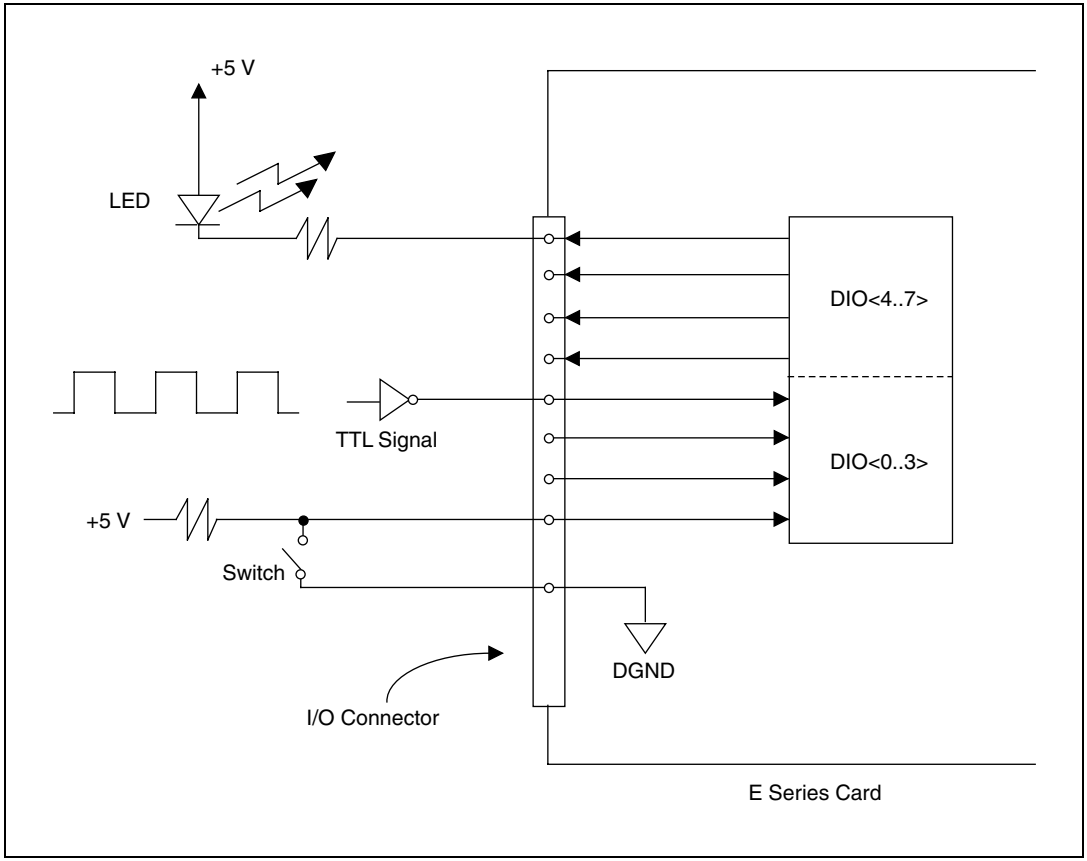


Figure 4-9. Digital I/O Connections

Figure 4-9 shows DIO<0..3> configured for digital input, and DIO<4..7> configured for digital output. Digital input applications include receiving TTL signals and sensing external device states such as the state of the switch shown in the figure. Digital output applications include sending TTL signals and driving external devices such as the LED shown in the figure.

Power Connections

Two pins on the I/O connector supply +5 V from the computer power supply through a self-resetting fuse. The fuse will reset automatically within a few seconds after the overcurrent condition is removed. These pins are referenced to DGND and can be used to power external digital circuitry.

Refer to the power requirement of the I/O connection supply in Appendix A, *Specifications*, for more information on powering your device.

Warning Do *not*, under any circumstances, connect these +5 V power pins directly to analog or digital ground or to any other voltage source on the DAQCard-6062E or any other device. Doing so can damage the DAQCard-6062E and the computer. National Instruments is *not* liable for damages resulting from such a connection.

Timing Connections

Warning Exceeding the maximum input voltage ratings, which are listed in Table 4-2, can damage the DAQCard-6062E and the computer. National Instruments in *not* liable for any damages resulting from such signal connections.

All external control over the timing of your DAQCard-6062E is routed through the 10 programmable function inputs labeled PFI0 through PFI9. These signals are explained in detail in the *Programmable Function Input Connections* section. These PFIs are bidirectional; as outputs they are not programmable and reflect the state of many data acquisition, waveform generation, and general-purpose timing signals. There are five other dedicated outputs for the remainder of the timing signals. As inputs, the PFI signals are programmable and can control any data acquisition, waveform generation, and general-purpose timing signals.

The *Data Acquisition Timing Connections* section explains the data acquisition signals. The *General-Purpose Timing Signal Connections* section explains the general-purpose timing signals.

All digital timing connections are referenced to DGND. This reference is demonstrated in Figure 4-10, which shows how to connect an external TRIG1 source and an external CONVERT* source to two of the DAQCard-6062E PFI pins.

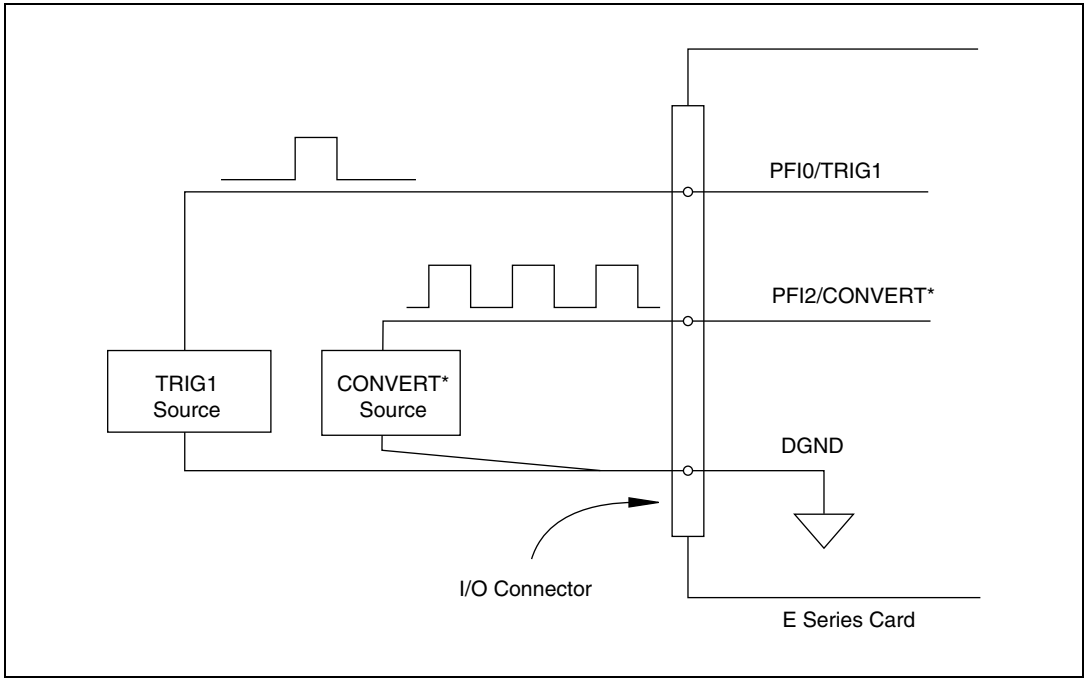


Figure 4-10. Timing I/O Connections

Programmable Function Input Connections

You can externally control a total of 13 internal timing signals from the PFI pins. The source for each of these signals is software selectable from any of the PFIs when you want external control. This flexible routing scheme reduces the need to change the physical wiring to the DAQCard-6062E I/O connector for different applications requiring alternative wiring.

You can individually enable each of the PFI pins to output a specific internal timing signal. For example, if you need the CONVERT* signal as an output on the I/O connector, software can turn on the output driver for the PFI2/CONVERT* pin. Be careful not to drive a PFI signal externally when it is configured as an output.

As an input, you can individually configure each PFI for edge or level detection and for polarity selection, as well. You can use the polarity selection for any of the 13 timing signals, but the edge or level detection will depend upon the particular timing signal being controlled. The detection requirements for each timing signal are listed within the section that discusses that individual signal.

In edge-detection mode, the minimum pulse width required is 10 ns. This requirement applies for both rising-edge and falling-edge polarity settings. Edge-detection mode does not have a maximum pulse-width requirement.

In level-detection mode, no minimum or maximum pulse-width requirements are imposed by the PFIs themselves, but limits may be imposed by the particular timing signal being controlled. These requirements are listed later in this chapter.

Data Acquisition Timing Connections

The data acquisition timing signals are SCANCLK, EXTSTROBE*, TRIG1, TRIG2, STARTSCAN, CONVERT*, AIGATE, and SISOURCE.

Posttriggered data acquisition allows you to view only data that is acquired after a trigger event is received. A typical posttriggered data acquisition sequence is shown in Figure 4-11. Pretriggered data acquisition allows you to view data that is acquired before the trigger of interest in addition to data acquired after the trigger. Figure 4-12 shows a typical pretriggered data acquisition sequence. The description for each signal shown in these figures is included later in this chapter.

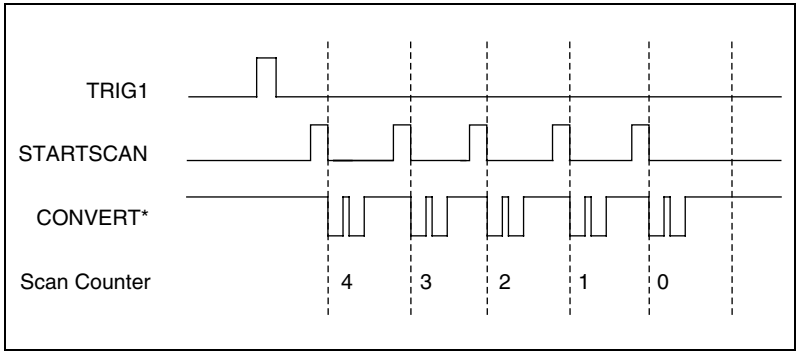


Figure 4-11. Typical Posttriggered Acquisition

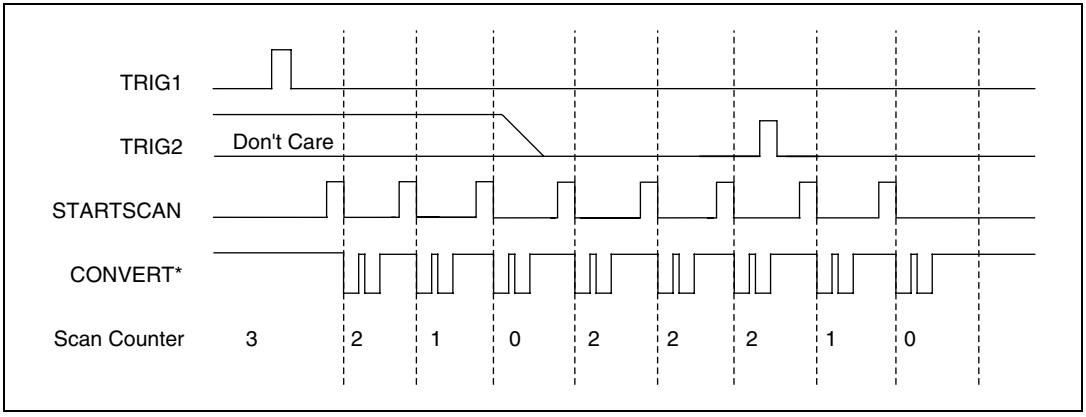


Figure 4-12. Typical Pretriggered Acquisition

SCANCLK Signal

SCANCLK is an output-only signal that generates a pulse with the leading edge occurring approximately 50 to 100 ns after an A/D conversion begins. The polarity of this output is software-selectable but is typically configured so that a low-to-high leading edge can clock external analog input multiplexers indicating when the input signal has been sampled and can be removed. This signal has a 400 to 500 ns pulse width and is software enabled. Figure 4-13 shows the timing for the SCANCLK signal.

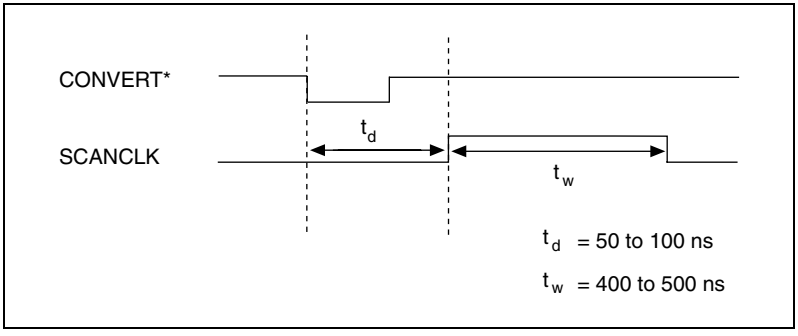


Figure 4-13. SCANCLK Signal Timing

EXTSTROBE* Signal

EXTSTROBE* is an output-only signal that generates either a single pulse or a sequence of eight pulses in the hardware-strobe mode. An external device can use this signal to latch signals or to trigger events. In the single-pulse mode, software controls the level of the EXTSTROBE* signal. Both 10 µs and 1.2 µs clocks are available for generating a sequence of eight pulses in the hardware-strobe mode. Figure 4-14 shows the timing for the hardware-strobe mode EXTSTROBE* signal.

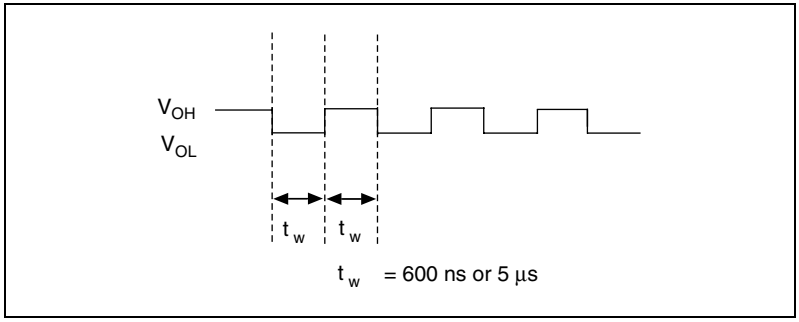


Figure 4-14. EXTSTROBE* Signal Timing

TRIG1 Signal

Any PFI pin can externally input the TRIG1 signal, which is available as an output on the PFI0/TRIG1 pin.

Refer to Figures 4-11 and 4-12 for the relationship of TRIG1 to the data acquisition sequence.

As an input, the TRIG1 signal is configured in the edge-detection mode. You can select any PFI pin as the source for TRIG1 and configure the polarity selection for either rising or falling edge. The selected edge of the TRIG1 signal starts the data acquisition sequence for both posttriggered and pretriggered acquisitions. The DAQCard-6062E supports analog triggering on the PFI0/TRIG1 pin. See Chapter 3, *Hardware Overview*, for more information on analog triggering.

As an output, the TRIG1 signal reflects the action that initiates a data acquisition sequence. This is true even if the acquisition is being externally triggered by another PFI. The output is an active high pulse with a pulse width of 50 to 100 ns. This output is set to tri-state at startup.

Figures 4-15 and 4-16 show the input and output timing requirements for the TRIG1 signal.

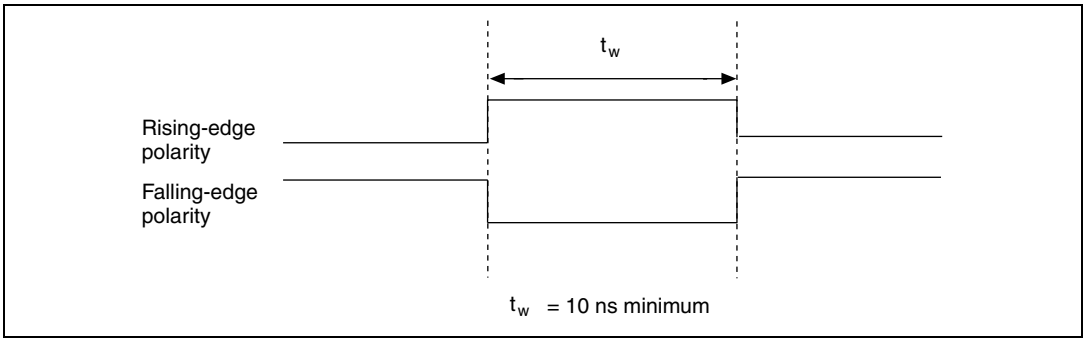


Figure 4-15. TRIG1 Input Signal Timing

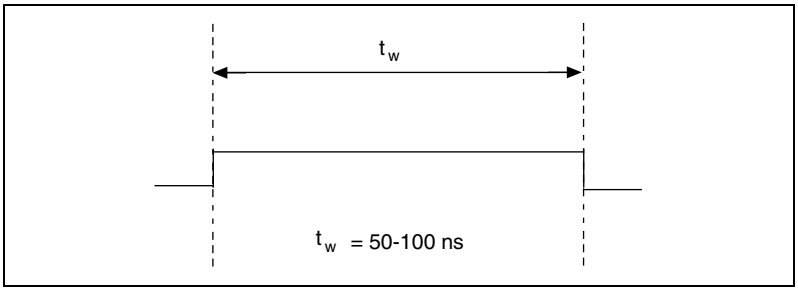


Figure 4-16. TRIG1 Output Signal Timing

The DAQCard-6062E also uses the TRIG1 signal to initiate pretriggered data acquisition operations. In most pretriggered applications, the TRIG1 signal is generated by a software trigger. Refer to the TRIG2 signal description for a complete description of the use of TRIG1 and TRIG2 in a pretriggered data acquisition operation.

TRIG2 Signal

Any PFI pin can externally input the TRIG2 signal, which is available as an output on the PFI1/TRIG2 pin.

Refer to Figure 4-12 for the relationship of TRIG2 to the data acquisition sequence.

As an input, the TRIG2 signal is configured in the edge-detection mode. You can select any PFI pin as the source for TRIG2 and configure the polarity selection for either rising or falling edge. The selected edge

of the TRIG2 signal initiates the posttriggered phase of a pretriggered acquisition sequence. In pretriggered mode, the TRIG1 signal initiates the data acquisition. The scan counter indicates the minimum number of scans before TRIG2 can be recognized. After the scan counter decrements to zero, it is loaded with the number of posttrigger scans to acquire while the acquisition continues. The DAQCard-6062E ignores the TRIG2 signal if it is asserted prior to the scan counter decrementing to zero. After the selected edge of TRIG2 is received, the DAQCard-6062E acquires a fixed number of scans and the acquisition stops. This mode acquires data both before and after receiving TRIG2.

As an output, the TRIG2 signal reflects the posttrigger in a pretriggered acquisition sequence. This is true even if the acquisition is being externally triggered by another PFI. The TRIG2 signal is not used in posttriggered data acquisition. The output is an active high pulse with a pulse width of 50 to 100 ns. This signal is set to input (High-Z) at startup.

Figures 4-17 and 4-18 show the input and output timing requirements for the TRIG2 signal.

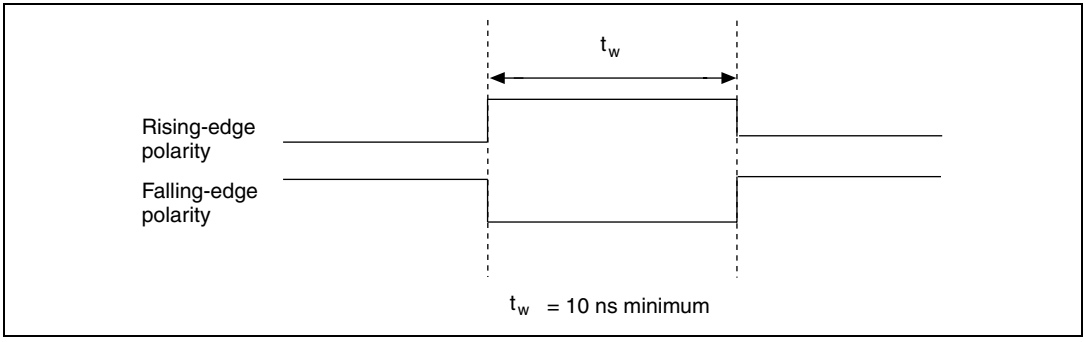


Figure 4-17. TRIG2 Input Signal Timing

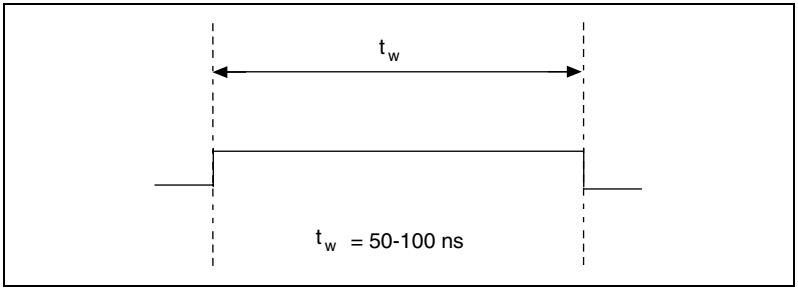


Figure 4-18. TRIG2 Output Signal Timing

STARTSCAN Signal

Any PFI pin can externally input the STARTSCAN signal, which is available as an output on the PFI7/STARTSCAN pin.

Refer to Figures 4-11 and 4-12 for the relationship of STARTSCAN to the data acquisition sequence.

As an input, the STARTSCAN signal is configured in the edge-detection mode. You can select any PFI pin as the source for STARTSCAN and configure the polarity selection for either rising or falling edge. The selected edge of the STARTSCAN signal initiates a scan. The sample interval counter is started if you select internally triggered CONVERT*.

As an output, the STARTSCAN signal reflects the actual start pulse that initiates a scan. This is true even if the starts are externally triggered by another PFI. You have two output options. The first option is an active high pulse with a pulse width of 50 to 100 ns, which indicates the start of the scan. The second option is an active high pulse that terminates at the start of the last conversion in the scan, which indicates a scan in progress. STARTSCAN will be deasserted t_{off} after the last conversion in the scan is initiated. This output is set to tri-state at startup.

Figures 4-19 and 4-20 show the input and output timing requirements for the STARTSCAN signal.

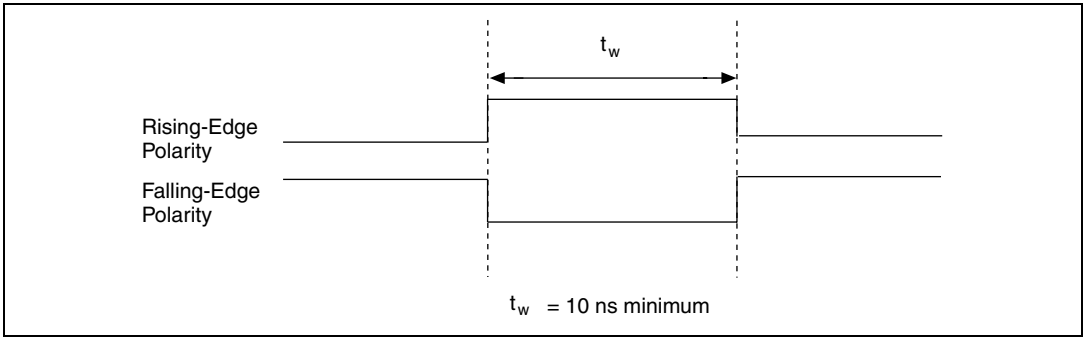


Figure 4-19. STARTSCAN Input Signal Timing

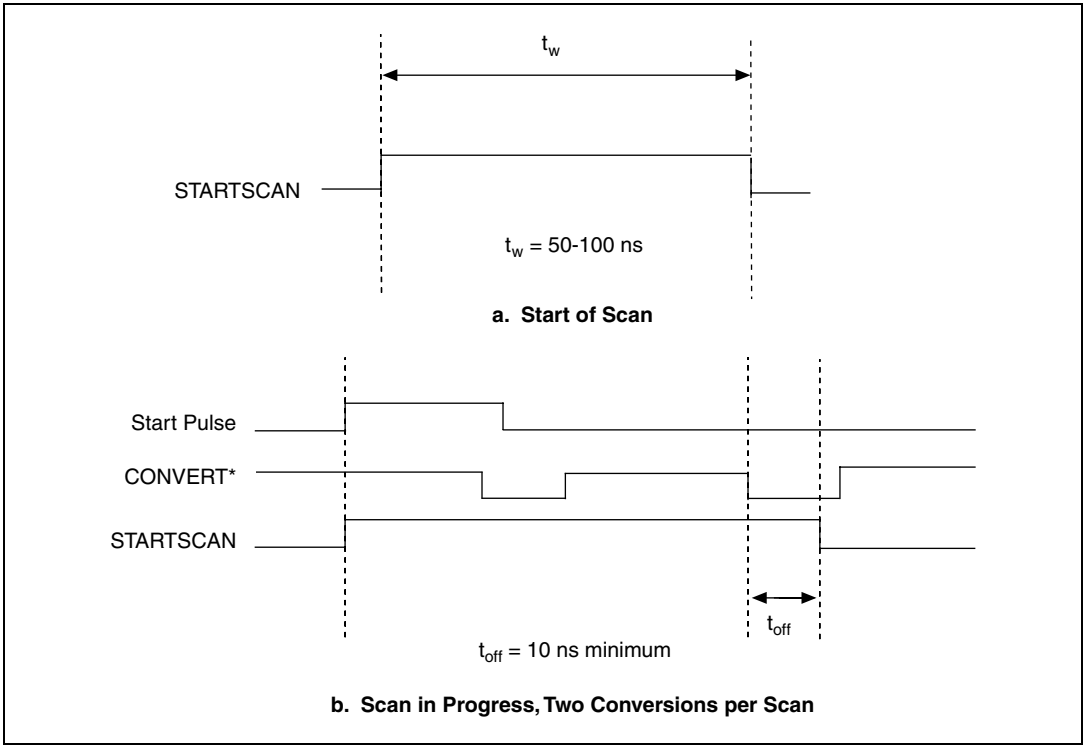


Figure 4-20. STARTSCAN Output Signal Timing

The CONVERT* pulses are masked off until the DAQCard-6062E generates the STARTSCAN signal. If you are using internally generated conversions, the first CONVERT* will appear when the onboard sample interval counter reaches zero. If you select an external CONVERT*, the first external pulse after STARTSCAN will generate a conversion. The STARTSCAN pulses should be separated by at least one scan period.

A counter on your DAQCard-6062E internally generates the STARTSCAN signal unless you select some external source. This counter is started by the TRIG1 signal and is stopped either by software or by the sample counter.

Scans generated by either an internal or external STARTSCAN signal are inhibited unless they occur within a data acquisition sequence. Scans occurring within a data acquisition sequence may be gated by either the hardware (AIGATE) signal or software command register gate.

CONVERT* Signal

Any PFI pin can externally input the CONVERT* signal, which is available as an output on the PFI2/CONVERT* pin.

Refer to Figures 4-11 and 4-12 for the relationship of STARTSCAN to the data acquisition sequence.

As an input, the CONVERT* signal is configured in the edge-detection mode. You can select any PFI pin as the source for CONVERT* and configure the polarity selection for either rising or falling edge. The selected edge of the CONVERT* signal initiates an A/D conversion.

As an output, the CONVERT* signal reflects the actual convert pulse that is connected to the ADC. This is true even if the conversions are externally generated by another PFI. The output is an active low pulse with a pulse width of 50 to 100 ns. This signal is set to input (High-Z) at startup.

Figures 4-21 and 4-22 show the input and output timing requirements for the CONVERT* signal.

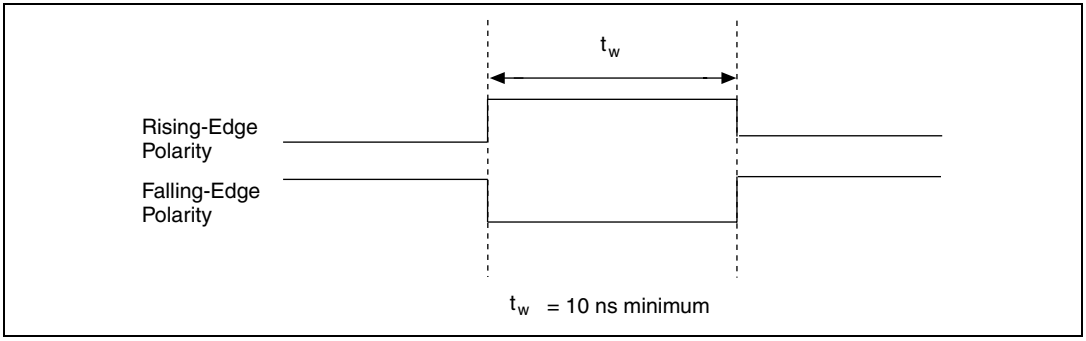


Figure 4-21. CONVERT* Input Signal Timing

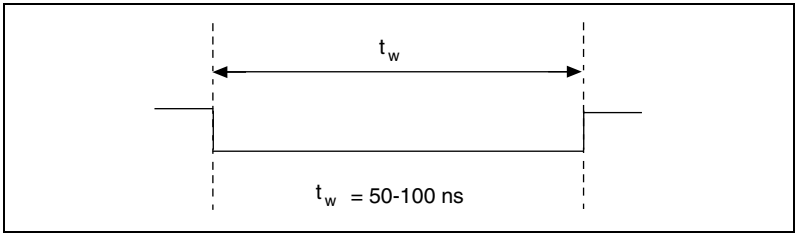


Figure 4-22. CONVERT* Output Signal Timing

The ADC switches to hold mode within 60 ns of the selected edge. This hold-mode delay time is a function of temperature and does not vary from one conversion to the next. Separate the CONVERT* pulses by at least one conversion period.

The sample interval counter on the DAQCard-6062E normally generates the CONVERT* signal unless you select some external source. The counter is started by the STARTSCAN signal and continues to count down and reload itself until the scan is finished. It then reloads itself in readiness for the next STARTSCAN pulse.

A/D conversions generated by either an internal or external CONVERT* signal are inhibited unless they occur within a data acquisition sequence. Scans occurring within a data acquisition sequence may be gated by either the hardware (AIGATE) signal or software command register gate.

AIGATE Signal

Any PFI pin can externally input the AIGATE signal, which is not available as an output on the I/O connector. The AIGATE signal can mask off scans in a data acquisition sequence. You can configure the PFI pin you select as the source for the AIGATE signal in either the level-detection or edge-detection mode. You can configure the polarity selection for the PFI pin for either active high or active low.

In the level-detection mode if AIGATE is active, the STARTSCAN signal is masked off, and no scans can occur. In the edge-detection mode, the first active edge disables the STARTSCAN signal, and the second active edge enables STARTSCAN.

The AIGATE signal can neither stop a scan in progress nor continue a previously gated-off scan; in other words, once a scan has started, AIGATE does not gate-off conversions until the beginning of the next scan and, conversely, if conversions are being gated off, AIGATE does not gate them back on until the beginning of the next scan.

SISOURCE Signal

Any PFI pin can externally input the SISOURCE signal, which is not available as an output on the I/O connector. The onboard scan interval counter uses the SISOURCE signal as a clock to time the generation of the STARTSCAN signal. You must configure the PFI pin you select as the source for the SISOURCE signal in the level-detection mode. You can configure the polarity selection for the PFI pin for either active high or active low.

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency limitation.

Either the 20 MHz or 100 kHz internal timebase generates the SISOURCE signal unless you select some external source. Figure 4-23 shows the timing requirements for the SISOURCE signal.

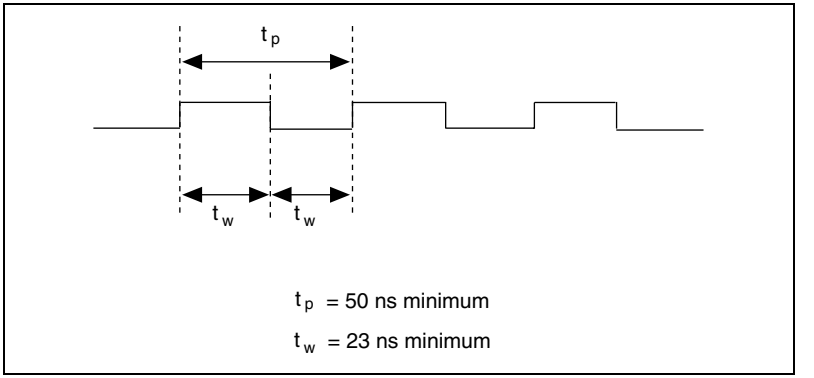


Figure 4-23. SISOURCE Signal Timing

Waveform Generation Timing Connections

The analog group defined for your DAQCard-6062E is controlled by WFTRIG, UPDATE*, and UISOURCE.

WFTRIG Signal

Any PFI pin can externally input the WFTRIG signal, which is available as an output on the PFI6/WFTRIG pin.

As an input, the WFTRIG signal is configured in the edge-detection mode. You can select any PFI pin as the source for WFTRIG and configure the polarity selection for either rising or falling edge. The selected edge of the WFTRIG signal starts the waveform generation for the DACs. The update interval (UI) counter is started if you select internally generated UPDATE*.

As an output, the WFTRIG signal reflects the trigger that initiates waveform generation. This is true even if the waveform generation is being externally triggered by another PFI. The output is an active high pulse with a pulse width of 50 to 100 ns. This output is set to tri-state at startup.

Figures 4-24 and 4-25 show the input and output timing requirements for the WFTRIG signal.

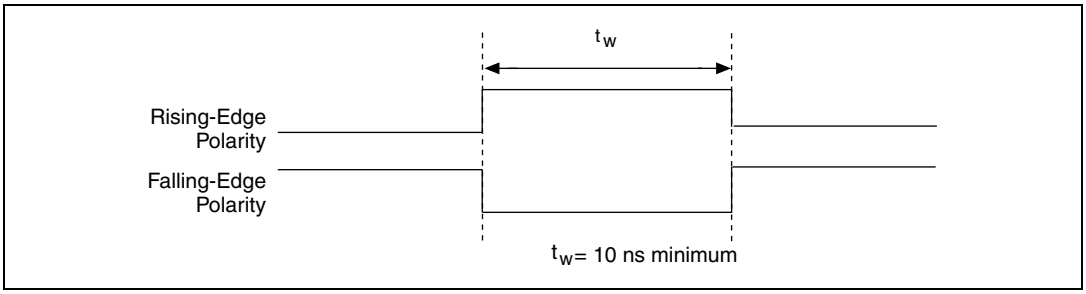


Figure 4-24. WFTRIG Input Signal Timing

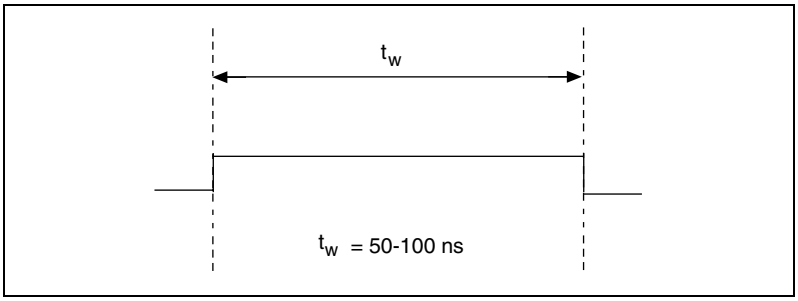


Figure 4-25. WFTRIG Output Signal Timing

UPDATE* Signal

Any PFI pin can externally input the UPDATE* signal, which is available as an output on the PFI5/UPDATE* pin.

As an input, the UPDATE* signal is configured in the edge-detection mode. You can select any PFI pin as the source for UPDATE* and configure the polarity selection for either rising or falling edge. The selected edge of the UPDATE* signal updates the outputs of the DACs. In order to use UPDATE*, you must set the DACs to posted-update mode.

As an output, the UPDATE* signal reflects the actual update pulse that is connected to the DACs. This is true even if the updates are being externally generated by another PFI. The output is an active low pulse with a pulse width of 300 to 350 ns. This output is set to tri-state at startup.

Figures 4-26 and 4-27 show the input and output timing requirements for the UPDATE* signal.

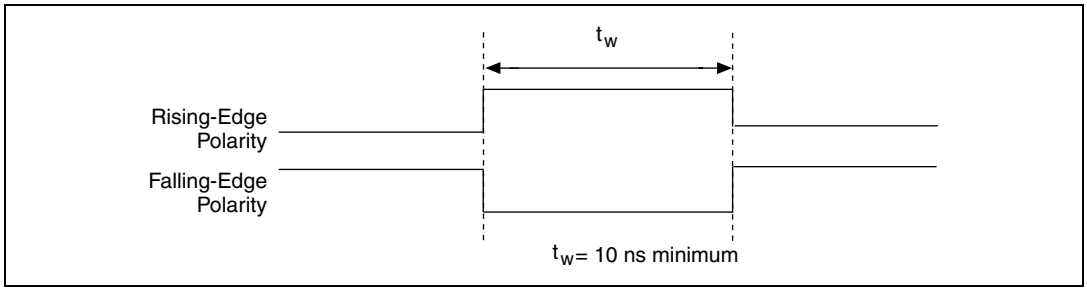


Figure 4-26. UPDATE* Input Signal Timing

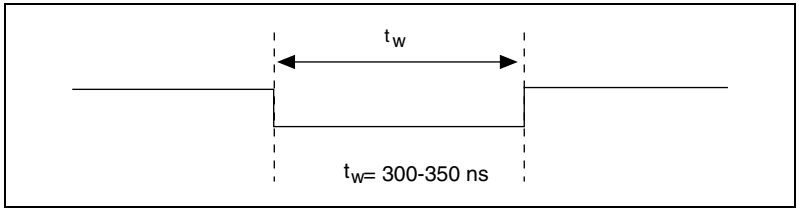


Figure 4-27. UPDATE* Output Signal Timing

The DACs are updated within 1.3 µs of the leading edge. Separate the UPDATE* pulses with enough time that new data can be written to the DAC latches.

The UI counter normally generates the UPDATE* signal unless you select some external source. The UI counter is started by the WFTRIG signal and can be stopped by software or the internal Buffer Counter.

D/A conversions generated by either an internal or external UPDATE* signal do not occur when gated by the software command register gate.

UISOURCE Signal

Any PFI pin can externally input the UISOURCE signal, which is not available as an output on the I/O connector. The UI counter uses the UISOURCE signal as a clock to time the generation of the UPDATE* signal. You must configure the PFI pin you select as the source for the UISOURCE signal in the level-detection mode. You can configure the

polarity selection for the PFI pin for either active high or active low. Figure 4-28 shows the timing requirements for the UISOURCE signal.

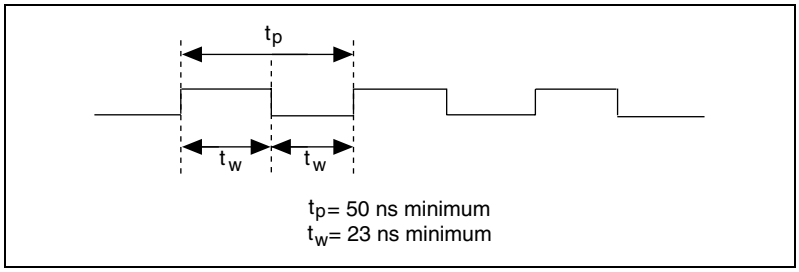


Figure 4-28. UISOURCE Signal Timing

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency limitation.

Either the 20 MHz or 100 kHz internal timebase normally generates the UISOURCE signal unless you select some external source.

General-Purpose Timing Signal Connections

The general-purpose timing signals are GPCTR0_SOURCE, GPCTR0_GATE, GPCTR0_OUT, GPCTR0_UP_DOWN, GPCTR1_SOURCE, GPCTR1_GATE, GPCTR1_OUT, GPCTR1_UP_DOWN, and FREQ_OUT.

GPCTR0_SOURCE Signal

Any PFI pin can externally input the GPCTR0_SOURCE signal, which is available as an output on the PFI8/GPCTR0_SOURCE pin.

As an input, the GPCTR0_SOURCE signal is configured in the edge-detection mode. You can select any PFI pin as the source for GPCTR0_SOURCE and configure the polarity selection for either rising or falling edge.

As an output, the GPCTR0_SOURCE signal reflects the actual clock connected to general-purpose counter 0. This is true even if another PFI is externally inputting the source clock. This signal is set to input (High-Z) at startup.

Figure 4-29 shows the timing requirements for the GPCTR0_SOURCE signal.

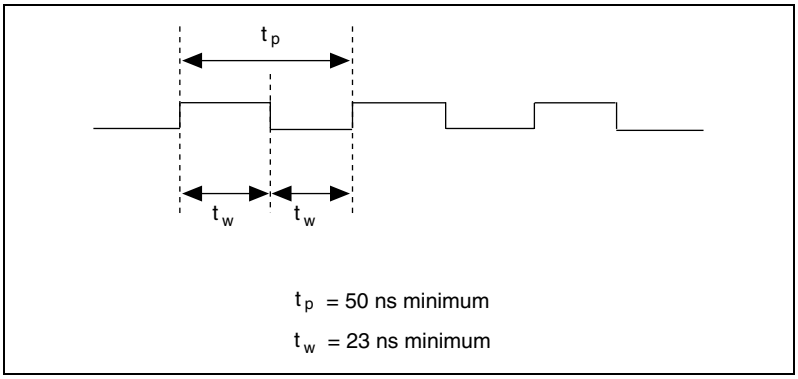


Figure 4-29. GPCTR0_SOURCE Signal Timing

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency limitation.

The 20 MHz or 100 kHz timebase normally generates the GPCTR0_SOURCE signal unless you select some external source.

GPCTR0_GATE Signal

Any PFI pin can externally input the GPCTR0_GATE signal, which is available as an output on the PFI9/GPCTR0_GATE pin.

As an input, the GPCTR0_GATE signal is configured in the edge-detection mode. You can select any PFI pin as the source for GPCTR0_GATE and configure the polarity selection for either rising or falling edge. You can use the gate signal in a variety of different applications to perform actions such as starting and stopping the counter, generating interrupts, saving the counter contents, and so on.

As an output, the GPCTR0_GATE signal reflects the actual gate signal connected to general-purpose counter 0. This is true even if the gate is being externally generated by another PFI. This signal is set to input (High-Z) at startup.

Figure 4-30 shows the timing requirements for the GPCTR0_GATE signal.

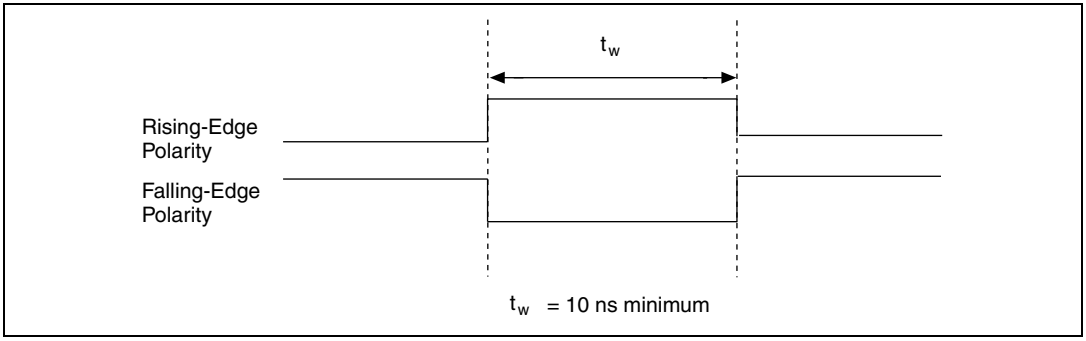


Figure 4-30. GPCTR0_GATE Signal Timing in Edge-Detection Mode

GPCTR0_OUT Signal

This signal is available only as an output on the GPCTR0_OUT pin. The GPCTR0_OUT signal reflects the terminal count (TC) of general-purpose counter 0. You have two software-selectable output options: pulse on TC and toggle output polarity on TC. The output polarity is software selectable for both options. This signal is set to input (High-Z) at startup. Figure 4-31 shows the timing of the GPCTR0_OUT signal.

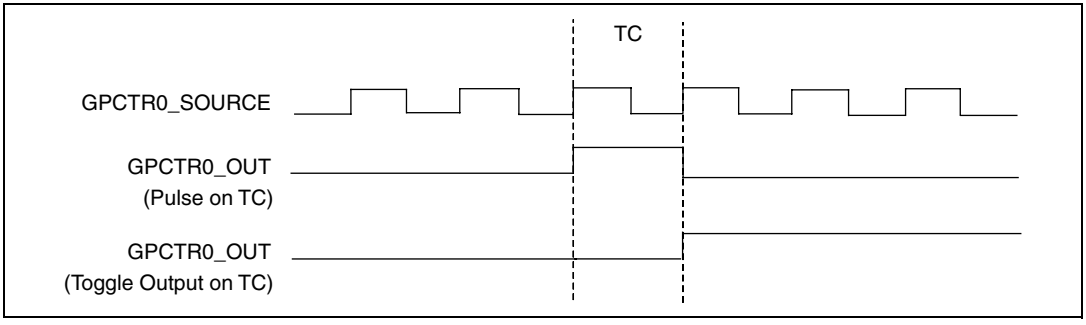


Figure 4-31. GPCTR0_OUT Signal Timing

GPCTR0_UP_DOWN Signal

This signal can be externally input on the DIO6 pin and is not available as an output on the I/O connector. The general-purpose counter 0 will count down when this pin is at a logic low and count up when it is at a logic high. You can disable this input so that software can control the up/down functionality and leave the DIO6 pin free for general use.

GPCTR1_SOURCE Signal

Any PFI pin can externally input the GPCTR1_SOURCE signal, which is available as an output on the PFI3/GPCTR1_SOURCE pin.

As an input, the GPCTR1_SOURCE signal is configured in the edge-detection mode. You can select any PFI pin as the source for GPCTR1_SOURCE and configure the polarity selection for either rising or falling edge.

As an output, the GPCTR1_SOURCE monitors the actual clock connected to general-purpose counter 1. This is true even if the source clock is being externally generated by another PFI. This signal is set to input (High-Z) at startup.

Figure 4-32 shows the timing requirements for the GPCTR1_SOURCE signal.

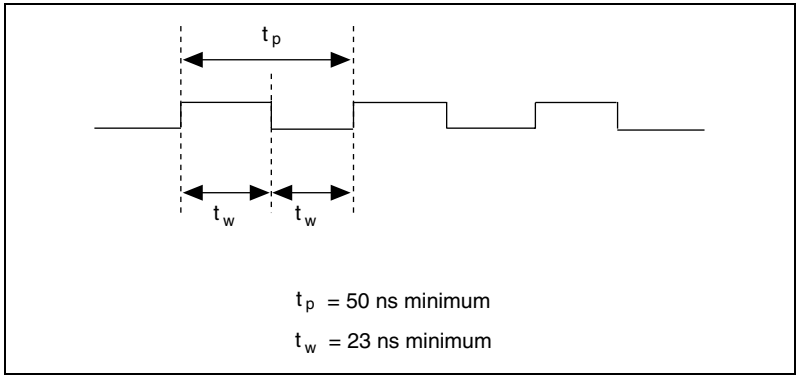


Figure 4-32. GPCTR1_SOURCE Signal Timing

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency limitation.

The 20 MHz or 100 kHz timebase normally generates the GPCTR1_SOURCE unless you select some external source.

GPCTR1_GATE Signal

Any PFI pin can externally input the GPCTR1_GATE signal, which is available as an output on the PFI4/GPCTR1_GATE pin.

As an input, the GPCTR1_GATE signal is configured in edge-detection mode. You can select any PFI pin as the source for GPCTR1_GATE and

configure the polarity selection for either rising or falling edge. You can use the gate signal in a variety of different applications to perform such actions as starting and stopping the counter, generating interrupts, saving the counter contents, and so on.

As an output, the GPCTR1_GATE signal monitors the actual gate signal connected to general-purpose counter 1. This is true even if the gate is being externally generated by another PFI. This signal is set to input (High-Z) at startup.

Figure 4-33 shows the timing requirements for the GPCTR1_GATE signal.

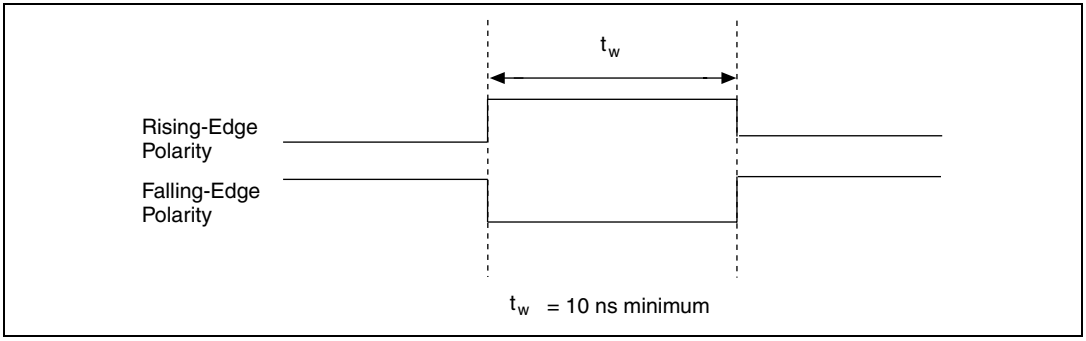


Figure 4-33. GPCTR1_GATE Signal Timing in Edge-Detection Mode

GPCTR1_OUT Signal

This signal is available only as an output on the GPCTR1_OUT pin. The GPCTR1_OUT signal monitors the TC board general-purpose counter 1. You have two software-selectable output options: pulse on TC and toggle output polarity on TC. The output polarity is software selectable for both options. This signal is set to input (High-Z) at startup. Figure 4-34 shows the timing requirements for the GPCTR1_OUT signal.

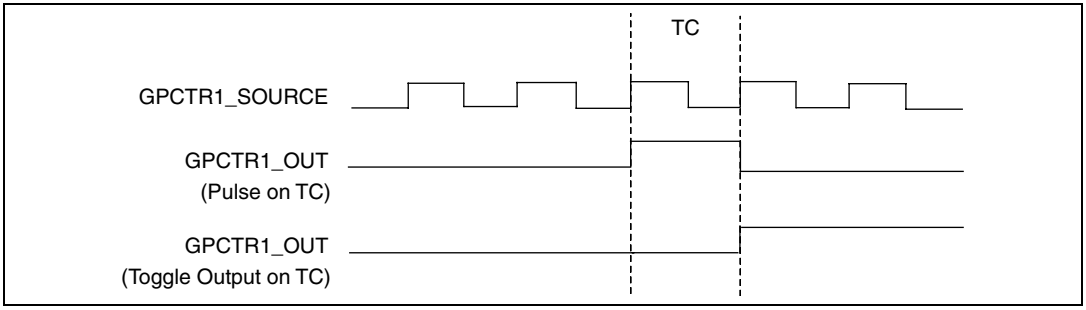
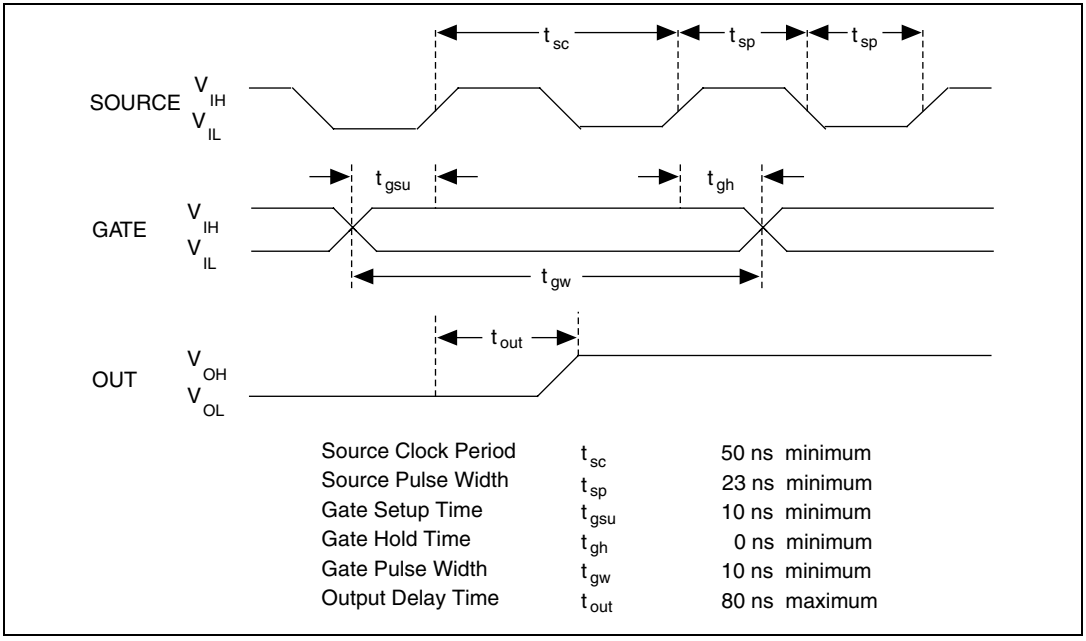


Figure 4-34. GPCTR1_OUT Signal Timing

GPCTR1_UP_DOWN Signal

This signal can be externally input on the DIO7 pin and is not available as an output on the I/O connector. General-purpose counter 1 counts down when this pin is at a logic low and counts up at a logic high. This input can be disabled so that software can control the up-down functionality and leave the DIO7 pin free for general use. Figure 4-35 shows the timing requirements for the GATE and SOURCE input signals and the timing specifications for the OUT output signals of your DAQCard-6062E.



Source Clock Period	t_{sc}	50 ns minimum
Source Pulse Width	t_{sp}	23 ns minimum
Gate Setup Time	t_{gsu}	10 ns minimum
Gate Hold Time	t_{gh}	0 ns minimum
Gate Pulse Width	t_{gw}	10 ns minimum
Output Delay Time	t_{out}	80 ns maximum

Figure 4-35. GPCTR Timing Summary

The GATE and OUT signal transitions shown in Figure 4-35 are referenced to the rising edge of the SOURCE signal. This timing diagram assumes that the counters are programmed to count rising edges. The same timing diagram, but with the source signal inverted and referenced to the falling edge of the source signal, would apply when the counter is programmed to count falling edges.

The GATE input timing parameters are referenced to the signal at the SOURCE input or to one of the internally generated signals on your DAQCard-6062E. Figure 4-35 shows the GATE signal referenced to the rising edge of a source signal. The gate must be valid (either high or low) for at least 10 ns before the rising or falling edge of a source signal for the gate to take effect at that source edge, as shown by t_{gsu} and t_{gh} in Figure 4-35. The gate signal is not required to be held after the active edge of the source signal.

If an internal timebase clock is used, the gate signal cannot be synchronized with the clock. In this case, gates applied close to a source edge take effect either on that source edge or on the next one. This arrangement results in an uncertainty of one source clock period with respect to unsynchronized gating sources.

The OUT output timing parameters are referenced to the signal at the SOURCE input or to one of the internally generated clock signals on the DAQCard-6062E. Figure 4-35 shows the OUT signal referenced to the rising edge of a source signal. Any OUT signal state changes occur within 80 ns after the rising or falling edge of the source signal.

FREQ_OUT Signal

This signal is available only as an output on the FREQ_OUT pin. The FREQ_OUT signal is the output of the DAQCard-6062E frequency generator. The frequency generator is a 4-bit counter that can divide its input clock by the numbers 1 through 16. The input clock of the frequency generator is software selectable from the internal 10 MHz and 100 kHz timebases. The output polarity is software selectable. This signal is set to input (High-Z) at startup.

Field Wiring Considerations

Environmental noise can seriously affect the accuracy of measurements made with your DAQCard-6062E if you do not take proper care when running signal wires between signal sources and the DAQCard-6062E. The following recommendations apply mainly to analog input signal routing to the DAQCard-6062E although they also apply to signal routing in general.

You can minimize noise pickup and maximize measurement accuracy by taking the following precautions:

- Use differential analog input connections to reject common-mode noise.
- Use individually shielded, twisted-pair wires to connect analog input signals to the DAQCard-6062E. With this type of wire, the signals attached to the CH+ and CH– inputs are twisted together and then covered with a shield. You then connect this shield only at one point to the signal source ground. This kind of connection is required for signals traveling through areas with large magnetic fields or high electromagnetic interference.
- Route signals to the DAQCard-6062E carefully. Keep cabling away from noise sources. The most common noise source in a computer data acquisition system is the video monitor. Separate the monitor from the analog signals as much as possible.

The following recommendations apply for all signal connections to your DAQCard-6062E:

- Separate DAQCard-6062E signal lines from high-current or high-voltage lines. These lines are capable of inducing currents in or voltages on the DAQCard-6062E signal lines if they run in parallel paths at a close distance. To reduce the magnetic coupling between lines, separate them by a reasonable distance if they run in parallel, or run the lines at right angles to each other.
- Do not run signal lines through conduits that also contain power lines.
- Protect signal lines from magnetic fields caused by electric motors, welding equipment, breakers, or transformers by running them through special metal conduits.

5

Calibration

This chapter discusses the calibration procedures for your DAQCard-6062E card. If you are using the NI-DAQ device driver, the software includes calibration functions for performing all of the steps in the calibration process.

Calibration refers to the process of minimizing measurement and output voltage errors by making small circuit adjustments. On the DAQCard-6062E, these adjustments take the form of writing values to onboard calibration DACs (CalDACs).

Some form of DAQCard-6062E calibration is required for all but the most forgiving applications. If no DAQCard-6062E calibration were performed, your signals and measurements could have very large offset, gain, and linearity errors.

Three levels of calibration are available to you, and these are described in this chapter. The first level is the fastest, easiest, and least accurate, whereas the last level is the slowest, most difficult, and most accurate.

Loading Calibration Constants

Your DAQCard-6062E is factory calibrated before shipment at approximately 25 °C to the levels indicated in Appendix A, *Specifications*. The associated calibration constants—the values that were written to the CalDACs to achieve calibration in the factory—are stored in the onboard nonvolatile memory (EEPROM). Because the CalDACs have no memory capability, they do not retain calibration information when the DAQCard-6062E is unpowered. Loading calibration constants refers to the process of loading the CalDACs with the values stored in the EEPROM. NI-DAQ software determines when this loading is necessary and does it automatically. If you are not using NI-DAQ, you must load these values yourself.

The EEPROM has a user-modifiable calibration area in addition to the permanent factory calibration area. This means that you can load the CalDACs with values either from the original factory calibration or from a calibration that you subsequently performed.

This method of calibration is not very accurate because it does not take into account the fact that the DAQCard-6062E measurement and output voltage errors can vary with time and temperature. It is better to self-calibrate when the DAQCard-6062E is installed in the environment in which it will be used.

Self-Calibration

Your DAQCard-6062E can measure and correct for almost all of its calibration-related errors without any external signal connections. Your National Instruments software provides a self-calibration method you can use. This self-calibration process, which generally takes less than a minute, is the preferred method of assuring accuracy in your application. Initiate self-calibration to minimize the effects of any offset, gain, and linearity drifts, particularly those effects due to warmup.

Immediately after self-calibration, the only significant residual calibration error could be gain error due to time or temperature drift of the onboard voltage reference. This error is addressed by external calibration, which is discussed in the following section. If you are interested primarily in relative measurements, you can ignore a small amount of gain error, and self-calibration should be sufficient.

External Calibration

Your DAQCard-6062E has an onboard calibration reference to ensure the accuracy of self-calibration. Its specifications are listed in Appendix A, *Specifications*. The reference voltage is measured at the factory and stored in the EEPROM for subsequent self-calibrations. This voltage is stable enough for most applications, but if you are using your DAQCard-6062E at an extreme temperature, or if the onboard reference has not been measured for a year or more, you may wish to externally calibrate your DAQCard-6062E.

An external calibration refers to calibrating your DAQCard-6062E with a known external reference rather than relying on the onboard reference. Redetermining the value of the onboard reference is part of this process and the results can be saved in the EEPROM, so you should not have to perform an external calibration very often. You can externally calibrate your DAQCard-6062E by calling the NI-DAQ calibration function.

To externally calibrate your DAQCard-6062E, use a very accurate external reference. The reference should be several times more accurate than the DAQCard-6062E itself. For example, to calibrate the 12-bit DAQCard-6062E, the external reference should be at least ±0.005% (±50 ppm) accurate.

Other Considerations

The CalDACs adjust the gain error of each analog output channel by adjusting the value of the reference voltage supplied to that channel. This calibration mechanism is designed to work only with the internal 10 V reference. Thus, in general, it is not possible to calibrate the analog output gain error when using an external reference. In this case, it is advisable to account for the nominal gain error of the analog output channel either in software or with external hardware. See Appendix A, *Specifications*, for analog output gain error information.

A

Specifications

This appendix lists the specifications of the DAQCard-6062E. These specifications are typical at 25 °C unless otherwise noted.

Analog Input

Input Characteristics

Number of channels ..... 16 single-ended,
16 pseudo-differential, or
8 differential (software-selectable on a per channel basis)

Type of ADC..... Successive approximation

Resolution ..... 12 bits, 1 in 4,096

Max sampling rate..... 500 kS/s

Input signal ranges

Board Gain (Software Selectable)	Board Range (Software Selectable)	
	Bipolar	Unipolar
0.5	±10 V	—
1	±5 V	0 to 10 V
2	±2.5 V	0 to 5 V
5	±1	0 to 2 V
10	±500 mV	0 to 1 V
20	±250 mV	0 to 500 mV
50	±100 mV	0 to 200 mV
100	±50 mV	0 to 100 mV

Input coupling.....DC

Max working voltage
(signal + common mode).....Each input should remain within ±11 V of ground

Overvoltage protection .....±25 V powered on, ±15 V powered off

Inputs protected .....ACH<0..15>, AISENSE

FIFO buffer size.....8,192 samples

Data transfers.....interrupt, programmed I/O

Configuration memory size .....512 words

Transfer Characteristics

Relative accuracy .....±0.5 LSB typ dithered, ±1.5 LSB max undithered

DNL.....–0.9, +1.5 LSB max

No missing codes.....12 bits, guaranteed

Offset error

Pregain error after calibration.....±16 µV max

Pregain error before calibration.....±4 mV max

Postgain error after calibration .....±1 mV max

Postgain error before calibration .....±265 mV max

Gain error (relative to calibration reference)

After calibration (gain = 1).....±0.02% of reading max

Before calibration .....±2.5% of reading max

Gain ≠ 1 with gain error adjusted to 0 at gain = 1 .....±0.02% of reading max

Amplifier Characteristics

Input impedance

Normal powered on ..... 100 GΩ in parallel with 100 pF

Powered off..... 820 Ω min

Overload..... 820 Ω min

Input bias current ..... ±200 pA

Input offset current..... ±100 pA

CMRR (all input ranges, DC to 60 Hz)

Gain ≤ 1 ..... 85 dB

Gain = 2 ..... 95 dB

Gain ≥ 5 ..... 100 dB

Dynamic Characteristics

Bandwidth

Small signal (–3 dB) ..... 1.3 MHz

Large signal (1% THD) ..... 300 kHz

Settling time for full-scale step

Gain	Accuracy	
	±0.012% (±0.5 LSB)	±0.024% (±1 LSB)
0.5	2.5 µs typ, 4 µs max	3 µs max

System noise in LSB rms, not including quantization

Gain	Noise, Dither Off	Noise, Dither On
0.5 to 10	0.45	0.70
20	0.50	0.75
50	0.65	0.8
100	0.9	1.0

Crosstalk (DC to 100 kHz) .....–75 dB (adjacent channels), –90 dB (all other channels), DC to 100 kHz

Stability

Offset temperature coefficient

Pregain.....±5 µV/°C

Postgain .....±240 µV/°C

Gain temperature coefficient .....±20 ppm/°C

Analog Output

Output Characteristics

Number of channels.....2 voltage

Resolution.....12 bits, 1 in 4,096

Max update rate

1 channel.....850 kS/s

2 channel.....850 kS/s

Type of DAC .....Double-buffered, multiplying

FIFO buffer size.....2,048 S

Data transfers.....interrupts, programmed I/O

Transfer Characteristics

Relative accuracy (INL)

After calibration.....±0.5 LSB typ, ±1.0 LSB max

Before calibration .....±4 LSB max

DNL

After calibration.....±0.5 LSB typ, ±1.0 LSB max

Before calibration .....±3 LSB max

Monotonicity .....12 bits, guaranteed after calibration

Offset error

- After calibration ..... ±1.0 mV max
- Before calibration ..... ±200 mV max

Gain error (relative to internal reference)

- After calibration ..... ±0.01% of output max
- Before calibration ..... ±0.7% of output max

Gain error (relative to external reference) ..... ±0.5% of output max, not adjustable

Voltage Output

Ranges ..... ±10 V, ±EXTREF, (software selectable)

Output coupling ..... DC

Output impedance ..... 0.1 Ω max

Current drive ..... ±5 mA max

Protection ..... Short-circuit to ground

Power-on state ..... 0 V

External reference input

- Range ..... ±11 V
- Overvoltage protection ..... ±25 V powered on, ±15 V powered off
- Input impedance ..... 10 kΩ
- Bandwidth (–3 dB) ..... 50 kHz

Dynamic Characteristics

Settling time for full-scale step ..... 3 µs to ±0.5 LSB accuracy

Slew rate ..... 20 V/µs

Noise ..... 200 µVrms, DC to 1 MHz

Glitch energy (at midscale transition)

Magnitude

Reglitching disabled.....±20 mV

Reglitching enabled.....±4 mV

Duration.....1.5 µs

Stability

Offset temperature coefficient.....±50 µV/°C

Gain temperature coefficient

Internal reference.....±25 ppm/°C

External reference.....±25 ppm/°C

Digital I/O

Number of channels.....8 input/output

Compatibility.....TTL/CMOS

Digital logic levels

Level	Min	Max
Input low voltage	0 V	0.8 V
Input high voltage	2 V	5 V
Input low current (V_{in} = 0 V)	—	–320 µA
Input high current (V_{in} = 5 V)	—	10 µA
Output low voltage (I_{OL} = 24 mA)	—	0.4 V
Output high voltage (I_{OH} = 13 mA)	4.35 V	—

Power-on state.....Input (High-Z)

Data transfers.....Programmed I/O

Timing I/O

Number of channels ..... 2 up/down counter/timers, 1 frequency scaler

Resolution

- Counter/timers ..... 24 bits
- Frequency scalers..... 4 bits

Compatibility ..... TTL/CMOS

Base clocks available

- Counter/timers ..... 20 MHz, 100 kHz
- Frequency scalers..... 10 MHz, 100 kHz

Base clock accuracy ..... ±0.01%

Max source frequency ..... 20 MHz

Min source pulse duration..... 10 ns in edge-detection mode

Min gate pulse duration..... 10 ns in edge-detection mode

Data transfers ..... interrupts, programmed I/O

Triggers

Analog Trigger

Source..... ACH<0..15>, external trigger (PFI0/TRIG1)

Level..... ± full-scale, internal; ±10 V, external

Slope..... Positive or negative (software selectable)

Resolution ..... 8 bits, 1 in 256

Hysteresis ..... Programmable

Bandwidth (–3 dB)..... 500 kHz internal, 2.5 MHz external

External input (PFI0/TRIG1)

Impedance.....12 kΩ

Coupling .....DC

Protection.....±35 V powered off,
–0.5 to VCC when configured as a digital signal,
±35 V when configured as an analog trigger signal or disabled

Digital Trigger

Compatibility .....TTL

Response .....Rising or falling edge

Pulse width .....10 ns min

Calibration

Recommended warm-up time.....15 min

Calibration interval .....1 year

External calibration reference.....>6 and <9.999 V

Onboard calibration reference

Level .....5.000 V (±2.5 mV)
(actual value stored in EEPROM)

Temperature coefficient.....±5 ppm/°C max

Long-term stability .....±15 ppm/$\sqrt{1,000\ \text{h}}$

Power Requirement (from PCMCIA I/O Channel)

+5 VDC (±5%)..... 330 mA typ in operational mode, 450 mA max in operational mode, 100 mA in power-down mode

Power available at I/O connector..... +4.65 to +5.25 V at 250 mA

Note These power usage figures do not include the power used by external devices that are connected to the fused supply present on the I/O connector.

Note also that under ordinary operation, the DAQCard has a current requirement of 320–350 mA; but if the analog inputs being sampled are overdriven at high gains, or if the analog inputs are left floating when the DAQCard is not in use, or if the analog outputs are loaded down, the current may increase to 450 mA.

Physical

PC card type..... Type II

I/O connector..... 68-position VHDCI female connector

Environment

Operating temperature..... 0 to 70 °C, internal device temperature as measured by internal termperature sensor

Storage temperature ..... –55 to 150 °C

Relative humidity..... 5 to 90% non-condensing

B

Optional Cable Connector Descriptions

This appendix describes the connectors on the optional cables for the DAQCard-6062E cards.

Figure B-1 shows the pin assignments for the 68-pin E series connector. This connector is available when you use the SHC68-68-EP cable assembly.

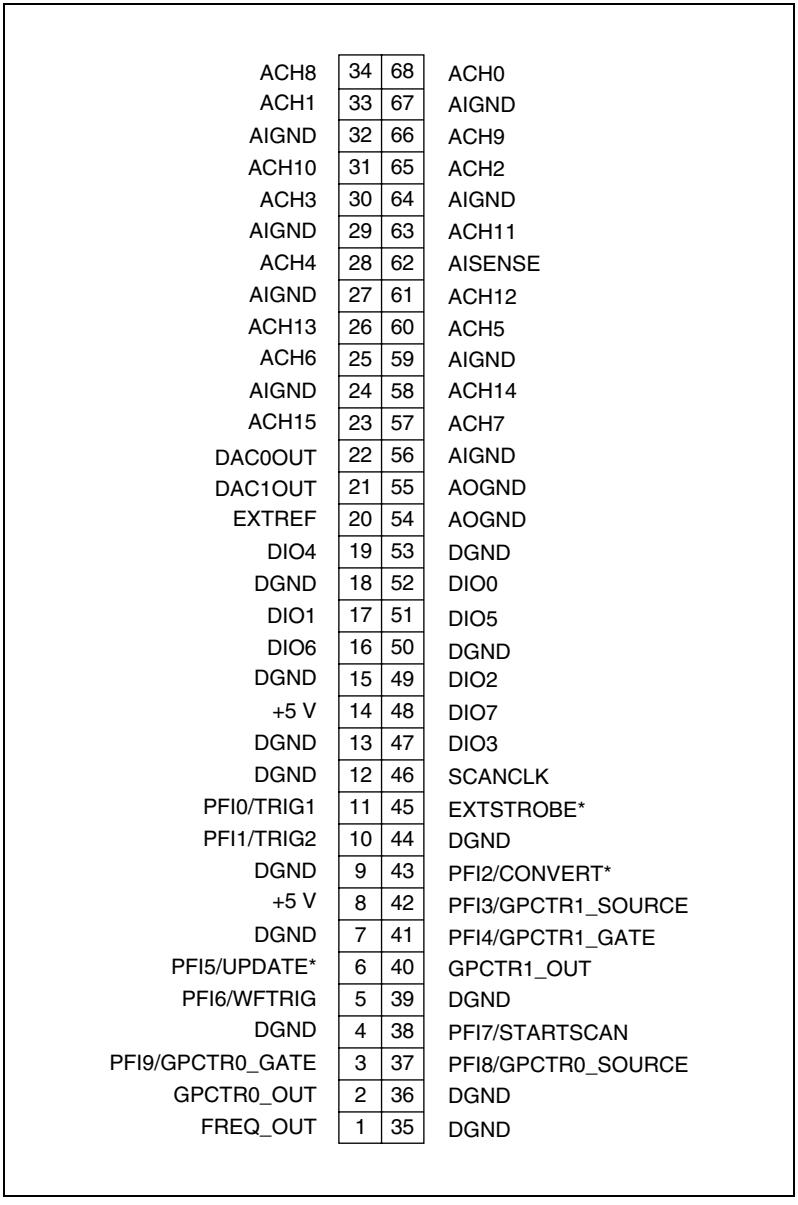


Figure B-1. 68-Pin E Series Connector Pin Assignments

Figure B-2 shows the pin assignments for the 50-pin E Series connector. This connector is available when you use the SHC68-68-EP cable assembly with the 68M-50F.

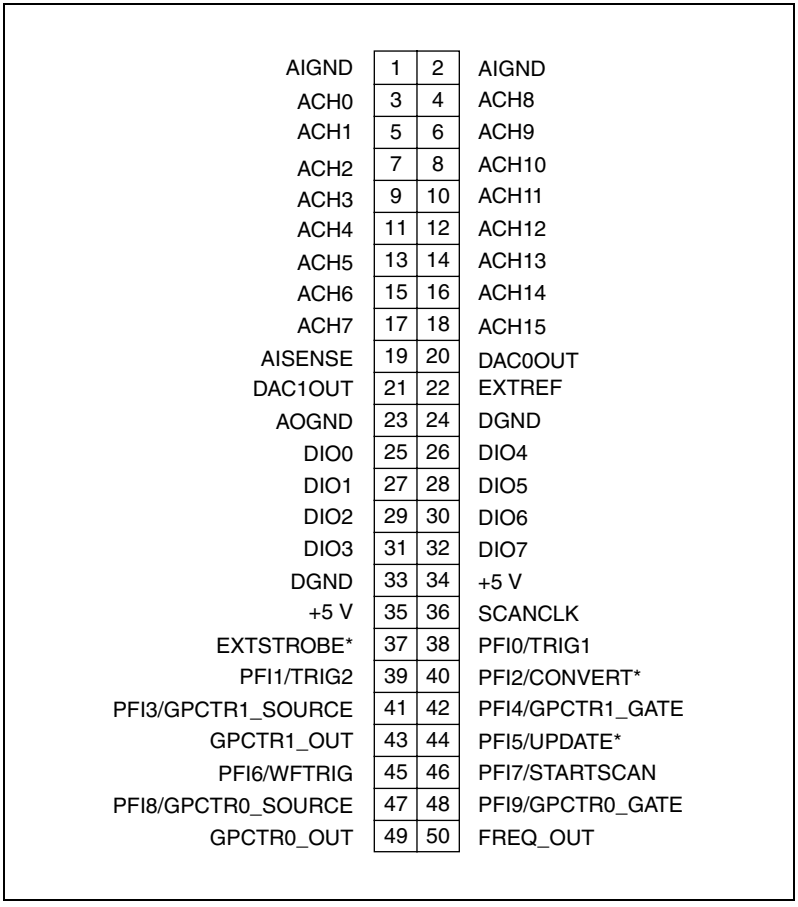


Figure B-2. 50-Pin E Series Connector Pin Assignments

C

Common Questions

This appendix contains a list of commonly asked questions and their answers relating to usage and special features of your DAQCard-6062E.

General Information

What is the DAQ-STC?

The DAQ-STC is the system timing control ASIC (application-specific integrated circuit) designed by National Instruments and is the backbone of the DAQCard-6062E. The DAQ-STC contains seven 24-bit counters and three 16-bit counters. The counters are divided into three groups:

- Analog input—two 24-bit, two 16-bit counters
- Analog output—three 24-bit, one 16-bit counters
- General-purpose counter/timer functions—two 24-bit counters

The groups can be configured independently with timing resolutions of 50 ns or 10 µs. With the DAQ-STC, you can interconnect a wide variety of internal timing signals to other internal blocks. The interconnection scheme is quite flexible and completely software configurable. New capabilities, such as buffered pulse generation, equivalent time sampling, and seamlessly changing the sampling rate, are possible.

What type of 5 V protection does the DAQCard-6062E have?

The DAQCard-6062E has 5 V lines equipped with a self-resetting 250 mA fuse.

Installation and Configuration

Which National Instruments documentation should I read first to get started using DAQ software?

Refer to the *Configuration* section in Chapter 2, *Installation and Configuration*, for this information.

What version of NI-DAQ must I have to program my DAQCard-6062E?

You must have version 6.7 or higher.

What is the best way to test my DAQCard without having to program the DAQCard?

If you are using Windows, Measurement & Automation Explorer has a **Test** menu with some excellent tools for doing simple functional tests of the DAQCard, such as analog input and output, digital I/O, and counter/timer tests.

Analog Input and Output

I'm using my DAQCard in differential analog input mode, and I have connected a differential input signal, but my readings are random and drift rapidly. What's wrong?

Check your ground-reference connections. Your signal may be referenced to a level that is considered *floating* with reference to the DAQCard ground reference. Even if you are in differential mode, the signal *must* still be referenced to the same ground level as the DAQCard reference. There are various methods of achieving the same ground level while maintaining a high common-mode rejection ratio (CMRR). These methods are outlined in Chapter 4, *Signal Connections*.

Can I sample across a number of channels on a DAQCard-6062E while each channel is being sampled at a different rate?

NI-DAQ features a function called `SCAN_Sequence_Setup`, which allows for multirate scanning of your analog input channels. Refer to the *NI-DAQ Function Reference Online Help* for more details.

I'm using the DACs to generate a waveform, but I discovered with a digital oscilloscope that there are glitches on the output signal. Is this normal?

When it switches from one voltage to another, any DAC produces glitches due to released charges. The largest glitches occur when the most significant bit (MSB) of the D/A code switches. A lowpass deglitching filter can help to remove some of these glitches, depending on the frequency and nature of your output signal. The DAQCard-6062E has built-in reglitchers, which can be software-enabled, on its analog output channels.

Can I synchronize a one-channel analog input data acquisition with a one-channel analog output waveform generation on my DAQCard-6062E?

Yes. One way to synchronize the channels is to use the waveform generation timing pulses to control the analog input data acquisition. To do this, follow steps 1 through 4 below, in addition to the usual steps for data acquisition and waveform generation configuration.

1. Enable the PFI5 line for output, as follows:
   - If you are using NI-DAQ, call `Select_Signal(deviceNumber, ND_PFI_5, ND_OUT_UPDATE, ND_HIGH_TO_LOW).`
   - If you are using LabVIEW, invoke Route Signal VI with signal name set to PFI5 and signal source set to AO Update.
2. Set up data acquisition timing so that the timing signal for A/D conversion comes from PFI5, as follows:
   - If you are using NI-DAQ, call `Select_Signal(deviceNumber, ND_IN_CONVERT, ND_PFI_5, ND_HIGH_TO_LOW).`
   - If you are using LabVIEW, invoke AI_Clock_Config_VI with clock source code set to PFI pin, high to low, and clock source string set to 5.
3. Initiate analog input data acquisition, which will start only when the analog output waveform generation starts.
4. Initiate analog output waveform generation.

Timing and Digital I/O

What types of triggering can be implemented in hardware on my DAQCard-6062E?

Digital and analog triggering are hardware-supported on the DAQCard-6062E.

Will the counter/timer applications that I wrote previously work with the DAQ-STC?

If you are using the NI-DAQ with LabVIEW, some of your applications drawn using the CTR VIs will still run. However, there are many differences in the counters between the DAQCard-6062E and other boards—the counter numbers are different; timebase selections are different; and the DAQ-STC counters are 24-bit counters (unlike the 16-bit counters on boards without the DAQ-STC).

If you are using the NI-DAQ language interface, such as LabWindows/CVI, the counter/time applications that you wrote previously will not work with the DAQ-STC. You must use the GPCTR functions; ICTR and CTR functions will not work with the DAQ-STC. The GPCTR functions have the same capabilities as the ICTR and CTR functions, plus more, but you must rewrite the application with the GPCTR function calls.

I'm using one of the general-purpose counter/timers on my DAQCard-6062E, but I do not see the counter/timer output on the I/O connector. What am I doing wrong?

If you are using the NI-DAQ language interface or LabWindows/CVI, you must configure the output line to output the signal to the I/O connector. Use the `Select_Signal` call in NI-DAQ to configure the output line. By default, all timing I/O lines except EXTSTROBE* are tri-stated.

What are the PFIs, and how do I configure these lines?

PFIs are Programmable Function Inputs. These lines serve as connections to virtually all internal timing signals.

If you are using NI-DAQ language interface, LabWindows, or LabWindows/CVI, use the `Select_Signal` function to route internal signals to the I/O connector, route external signals to internal timing sources, or tie internal timing signals together.

If you are using NI-DAQ with LabVIEW and you want to connect external signal sources to the PFI lines, you can use AI Clock Config, AI Trigger

Config, AO Clock Config, AO Trigger and Gate Config, CTR Mode Config, and CTR Pulse Config advanced level VIs to indicate which function the connected signal will serve. Use the Route Signal VI to enable the PFI lines to output internal signals.

Warning If you enable a PFI line for output, do not connect any external signal source to it; if you do, you can damage the DAQCard, the computer, and the connected equipment.

What are the power-on states of the PFI and DIO lines on the I/O connector?

At system power-on and reset, both the PFI and DIO lines are set to high impedance by the hardware. This setting means that the board circuitry is not actively driving the output either high or low. However, these lines may have pull-up or pull-down resistors connected to them as shown in Tables 4-1 and 4-2. These resistors weakly pull the output to either a logic high or logic low state. For example, DIO(0) will be in the high impedance state after power on, and Table 4-1 shows that there is a 50 kΩ pull-up resistor. This pull-up resistor will set the DIO(0) pin to a logic high when the output is in a high impedance state.

D

Technical Support Resources

This appendix describes the comprehensive resources available to you in the Technical Support section of the National Instruments Web site and provides technical support telephone numbers for you to use if you have trouble connecting to our Web site or if you do not have internet access.

NI Web Support

To provide you with immediate answers and solutions 24 hours a day, 365 days a year, National Instruments maintains extensive online technical support resources. They are available to you at no cost, are updated daily, and can be found in the Technical Support section of our Web site at `www.ni.com/support`

Online Problem-Solving and Diagnostic Resources

- **KnowledgeBase**—A searchable database containing thousands of frequently asked questions (FAQs) and their corresponding answers or solutions, including special sections devoted to our newest products. The database is updated daily in response to new customer experiences and feedback.
- **Troubleshooting Wizards**—Step-by-step guides lead you through common problems and answer questions about our entire product line. Wizards include screen shots that illustrate the steps being described and provide detailed information ranging from simple getting started instructions to advanced topics.
- **Product Manuals**—A comprehensive, searchable library of the latest editions of National Instruments hardware and software product manuals.
- **Hardware Reference Database**—A searchable database containing brief hardware descriptions, mechanical drawings, and helpful images of jumper settings and connector pinouts.
- **Application Notes**—A library with more than 100 short papers addressing specific topics such as creating and calling DLLs, developing your own instrument driver software, and porting applications between platforms and operating systems.

Software-Related Resources

- **Instrument Driver Network**—A library with hundreds of instrument drivers for control of standalone instruments via GPIB, VXI, or serial interfaces. You also can submit a request for a particular instrument driver if it does not already appear in the library.
- **Example Programs Database**—A database with numerous, non-shipping example programs for National Instruments programming environments. You can use them to complement the example programs that are already included with National Instruments products.
- **Software Library**—A library with updates and patches to application software, links to the latest versions of driver software for National Instruments hardware products, and utility routines.

Worldwide Support

National Instruments has offices located around the globe. Many branch offices maintain a Web site to provide information on local services. You can access these Web sites from `www.ni.com/worldwide`

If you have trouble connecting to our Web site, please contact your local National Instruments office or the source from which you purchased your National Instruments product(s) to obtain support.

For telephone support in the United States, dial 512 795 8248. For telephone support outside the United States, contact your local branch office:

Australia 03 9879 5166, Austria 0662 45 79 90 0, Belgium 02 757 00 20,
Brazil 011 284 5011, Canada (Calgary) 403 274 9391,
Canada (Ontario) 905 785 0085, Canada (Québec) 514 694 8521,
China 0755 3904939, Denmark 45 76 26 00, Finland 09 725 725 11,
France 01 48 14 24 24, Germany 089 741 31 30, Greece 30 1 42 96 427,
Hong Kong 2645 3186, India 91805275406, Israel 03 6120092,
Italy 02 413091, Japan 03 5472 2970, Korea 02 596 7456,
Mexico (D.F.) 5 280 7625, Mexico (Monterrey) 8 357 7695,
Netherlands 0348 433466, New Zealand 09 914 0488,
Norway 32 27 73 00, Poland 0 22 528 94 06, Portugal 351 1 726 9011,
Singapore 2265886, Spain 91 640 0085, Sweden 08 587 895 00,
Switzerland 056 200 51 51, Taiwan 02 2528 7227,
United Kingdom 01635 523545

Glossary

Prefix	Meanings	Value
p-	pico-	10^{-12}
n-	nano-	10^{-9}
µ-	micro-	10^{-6}
m-	milli-	10^{-3}
k-	kilo-	10^{3}
M-	mega-	10^{6}
G-	giga-	10^{9}

Symbols

°	degrees
–	negative of, or minus
Ω	ohms
/	per
%	percent
±	plus or minus
+	positive of, or plus
$\sqrt{\ }$	square root of
+5 V	+5 VDC source signal

A

A	amperes
AC	alternating current
ACH	analog input channel signal
A/D	analog-to-digital
ADC	analog-to-digital converter—an electronic device, often an integrated circuit, that converts an analog voltage to a digital number
ADIO	analog/digital input/output
AI	analog input
AIGATE	analog input gate signal
AIGND	analog input ground signal
AISENSE	analog input sense signal
AO	analog output
AOGND	analog output ground signal
ASIC	application-specific integrated circuit

B

BBS	bulletin board support
BIOS	basic input/output system or built-in operating system

C

C	Celsius
CalDAC	calibration DAC
CH	channel
CIS	Card Information Structure

cm	centimeter
CMOS	complementary metal-oxide semiconductor
CMRR	common-mode rejection ratio
CONVERT*	convert signal
CTR	counter

D

D/A	digital-to-analog
DAC	digital-to-analog converter—an electronic device, often an integrated circuit, that converts a digital number into a corresponding analog voltage or current
DAC0OUT	analog channel 0 output signal
DAC1OUT	analog channel 1 output signal
DAQ	data acquisition—a system that uses the computer to collect, receive, and generate electrical signals
DAQCard	data acquisition card
dB	decibel—the unit for expressing a logarithmic measure of the ratio of two signal levels: dB=20log10 V1/V2, for signals in volts
DC	direct current
DGND	digital ground signal
DIFF	differential
DIO	digital input/output
DMA	direct memory access—a method by which data can be transferred to/from computer memory from/to a device or memory on the bus while the processor does something else. DMA is the fastest method of transferring data to/from computer memory.
DNL	differential nonlinearity

DO	digital output
DOS	disk operating system

E

EEPROM	electrically erasable programmable read-only memory
EISA	Extended Industry Standard Architecture
EPROM	erasable programmable read-only memory
EXTREF	external reference signal
EXTSTROBE	external strobe signal

F

F	farads
FIFO	first-in first-out memory buffer—FIFOs are often used on DAQ devices to temporarily store incoming or outgoing data until that data can be read or written. For example, an analog input FIFO stores the results of A/D conversions until the data can be read into system memory. Programming the DMA controller and servicing interrupts can take several milliseconds in some cases. During this time, data accumulates in the FIFO for future retrieval. With a larger FIFO, longer latencies can be tolerated. In the case of analog output, a FIFO permits faster update rates, because the waveform data can be stored in the FIFO ahead of time. This again reduces the effect of latencies associated with getting the data from system memory to the DAQ device.
FREQ_OUT	frequency output signal
ft	feet

G

GATE	gate signal
GPCTR	general purpose counter

GPCTR0_GATE	general purpose counter 0 gate signal
GPCTR1_GATE	general purpose counter 1 gate signal
GPCTR0_OUT	general purpose counter 0 output signal
GPCTR1_OUT	general purpose counter 1 output signal
GPCTR0_SOURCE	general purpose counter 0 clock source signal
GPCTR1_SOURCE	general purpose counter 1 clock source signal
GPTR0_UP_DOWN	general purpose counter 0 up down signal
GPTR1_UP_DOWN	general purpose counter 1 up down signal

H

h	hour
hex	hexadecimal
Hz	hertz

I

ICTR	input counter
I/O	input/output—the transfer of data to/from a computer system involving communications channels, operator interface devices, and/or data acquisition and control interfaces
I_{OH}	current, output high
I_{OL}	current, output low
INL	relative accuracy
IRQ	interrupt request signal
ISA	Industry Standard Architecture

L

LED	light emitting diode
LSB	least significant bit

M

m	meter
MB	megabytes of memory
MIO	multifunction I/O
MSB	most significant bit

N

NC	not connected internally
NI-DAQ	NI driver software for DAQ hardware
NRSE	nonreferenced single-ended

O

OUT	output signal

P

PC	personal computer
PCI	Peripheral Component Interconnect—a high-performance expansion bus architecture originally developed by Intel to replace ISA and EISA. It is achieving widespread acceptance as a standard for PCs and work-stations; it offers a theoretical maximum transfer rate of 132 MB/s.
PCMCIA	Personal Computer Memory Card Association
PFI	Programmable Function Input

PFI0/TRIG1	PFI0/trigger 1
PFI1/TRIG2	PFI1/trigger 2
PFI2/CONVERT*	PFI2/convert
PFI3/GPCTR1_SOURCE	PFI3/general purpose counter 1 source
PFI4/GPCTR1_GATE	PFI4/general purpose counter 1 gate
PFI5/UPDATE*	PFI5/update
PFI6/WFTRIG	PFI6/waveform trigger
PFI7/STARTSCAN	PFI7/start of scan
PFI8/GPCTR0_SOURCE	PFI8/general purpose counter 0 source
PFI9/GPCTR0_GATE	PFI9/general purpose counter 0 gate
PGIA	Programmable Gain Instrumentation Amplifier
ppm	parts per million
pu	pullup
PWRDOWN	power down signal

R

RAM	random access memory
REF	reference
rms	root mean square
RSE	referenced single-ended
RTD	resistive temperature detector—a metallic probe that measures temperature based upon its coefficient of resistivity
RTSI	real-time system integration bus—the National Instruments timing bus that connects DAQ boards directly, by means of connectors on top of the boards, for precise synchronization of functions

S

s	seconds
S	samples
SCANCLK	scan clock signal
SCXI	Signal Conditioning eXtensions for Instrumentation—the National Instruments product line for conditioning low-level signals within an external chassis near sensors so only high-level signals are sent to DAQ boards in the noisy computer environment
SE	single-ended—a term used to describe an analog input that is measured with respect to a common ground
SISOURCE	SI counter clock signal
STARTSCAN	start scan signal

T

TC	terminal count signal
t_{gh}	gate hold time
t_{gsu}	gate setup time
t_{gw}	gate pulse width
THD	total harmonic distortion—the ratio of the total rms signal due to harmonic distortion to the overall rms signal, in dB or percent
t_{out}	output delay time
TRIG	trigger signal
t_{sc}	source clock period
t_{sp}	source pulse width
TTL	transistor-transistor logic

U

UI	update interval
UISOURCE	update interval counter clock signal
UPDATE*	update signal

V

V	volts
VCC	positive voltage supply
VDC	volts direct current
VI	virtual instrument—(1) a combination of hardware and/or software elements, typically used with a PC, that has the functionality of a classic stand-alone instrument (2) a LabVIEW software module (VI), which consists of a front panel user interface and a block diagram program
V_{IH}	volts, input high
V_{IL}	volts, input low
V_{in}	volts in
V_o	volts, output
V_{OH}	volts, output high
V_{OL}	volts, output low
V_{ref}	reference voltage

W

W	watts
waveform	multiple voltage readings taken at a specific sampling rate
WFTRIG	waveform generation trigger signal

Index

Numbers

A

B

C

D

E

F

G

H

I

L

M

N

O

P

Q

R

S

T

U

V

W